Universal Analogue Measurement and Signal-Conditioning Module

Theoretical Foundations and Study of the ESA Board

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Foreword

This report documents a one-week internship I carried out with Professor Antonio Selmo in his laboratory, during which I studied the theory of analogue signal amplification and conditioning as it is applied in an industrial setting. The theoretical content presented here was written by Professor Selmo; my work consisted of studying these principles, measuring the modules of the board, and understanding the design philosophy behind it.

These principles serve as the introduction to the Universal Transducer Conditioning board studied in the final chapter. The board was developed by Professor Selmo and is currently used by a European Space Agency laboratory in Padova, Italy.

I would like to take this opportunity to sincerely thank Professor Selmo for giving me the chance to complete this internship and study this material. Bonne lecture !

Authorship and contributions

Contributor	Contribution
Antonio Selmo	Author of the theoretical content of the report.
Matteo Avigni	Summer internship: study of the theoretical principles, measurement of the modules of the ESA board, and analysis of the design philosophy behind it.

Theoretical Foundations and Study of the ESA Board

Abstract

A measurement channel converts a physical quantity into an electrical signal, conditions that signal, and presents a voltage to acquisition. This report studies each functional module in sequence: the transducer, excitation and input interface, protection, range mapping, amplification, filtering, calibration, and output stage. For each module, it develops both the governing principle and the practical challenges that determine whether the measurement remains valid, including invertibility, loading, interference, headroom, offset, noise, bandwidth, stability, and drive capability.

The final chapter applies these concepts to the ESA board. It describes the selectable excitation, input, filtering, gain, reference, and output functions that form its configurable analogue channel.

Executive orientation

The theory begins with the complete measurement relationship, then examines the transducer law before deriving the mathematical range map required from the conditioning chain. The following chapters study the electrical interfaces and the individual analogue modules, together with the limitations and design choices that arise at each boundary. The ESA-board study then follows the same signal path from sensor excitation through the selected input mode, filter banks, gain and translation stages, and output driver.

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Nomenclature and abbreviations

Table 1. Principal notation and abbreviations.

Symbol or term	Meaning	Typical unit
x	Physical measurand	application-dependent
f_T	Transducer transfer characteristic	application-dependent
v_d	Differential input voltage, $v_P - v_N$	V
v_{cm}	Common-mode input voltage, $(v_P + v_N)/2$	V
G, G_1, G_2	Total or stage voltage gain	V/V
V_0, E_0	Additive translation or reference term	V
R_G	Instrumentation-amplifier gain-setting resistor	Ω
R_F	Feedback resistance	Ω
CMRR	Common-mode rejection ratio	ratio or dB
f_s	Sampling frequency	Hz
ADC	Analogue-to-digital converter	—
RTD	Resistance temperature detector	—

1.Measurement-chain synthesis

The report first establishes the end-to-end measurement relationship, then studies the individual modules, their interfaces, and the practical limits that determine whether the numerical result remains uniquely related to the original measurand.

1.1.From a physical quantity to usable measurement information

A measurement system does more than produce an electrical signal. It must preserve enough information about a physical quantity that the physical value can be reconstructed unambiguously and with a known error. The complete chain runs from the measurand $x(t)$ through the transducer to its electrical response $e_T(t)$, then through the conditioning electronics to the standardized output $v_o(t)$, and finally through the instrument or analogue-to-digital converter to the recovered value $\hat{x}(t)$.

The symbol x denotes the measurand, e_T the electrical quantity delivered by the transducer, v_o the standardized voltage supplied to the receiving instrument, and $\hat{x}$ the physical value recovered from the electrical measurement.

The transducer and conditioner must be considered together. A Pt100, for example, does not directly generate a convenient voltage. Its electrical property is resistance. An excitation circuit is therefore needed to turn the resistance into a voltage; the resulting millivolt-level signal must then be translated, amplified, filtered, and presented to the measuring instrument without corrupting the transducer's law.

The useful classifications are those that change the signal-chain design. A source may already produce voltage or current, or it may be parametric, as with a Pt100, which requires excitation. Its characteristic may be linear or nonlinear, but the decisive requirement is not strict linearity: over the selected range, each electrical output must correspond to exactly one physical input. The conditioned output may then be unipolar or bipolar according to the receiving instrument, fixing the required translation term.

Static behaviour defines the input-output curve and its errors; dynamic behaviour defines whether changes in time and useful spectral content are transferred faithfully. Connection distance matters as well: long leads make lead resistance and electromagnetic pickup part of the measurement problem, so two-wire and four-wire connections are different measurement architectures, not merely cabling choices.

These distinctions lead directly to the input, conditioning, and acquisition requirements.

The diagram in Figure 1 condenses the transducer relationship. The labels identify the principal physical quantity, the superposed influence quantities, the transducer and its electrical response. The manufacturer's forward rule maps the physical inputs to that response; the inverse rule used by the measurement system reconstructs the measurand within the declared operating range.

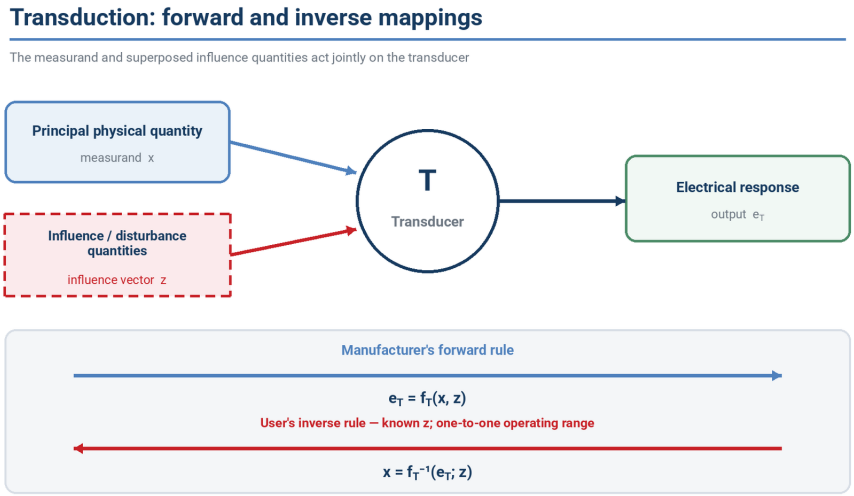


Figure 1. Transducer mapping between a principal physical quantity and its electrical response, including superposed influence quantities and the corresponding forward and inverse rules.

1.2.What the conditioning circuit must accomplish

The conditioner receives whatever electrical quantity the transducer naturally supplies and produces a voltage suitable for the measuring instrument. Its requirements are both static and dynamic.

The complete relationship between the measurand x and the conditioned output v_o must remain known and invertible. The conditioner must not introduce ambiguity, saturation, or an uncontrolled dependence on unwanted variables.

The output must also respect the instrument's accepted voltage range, for example 0 to $10\,\mathrm{V}$ or -5 to $+10\,\mathrm{V}$. It may be unipolar or bipolar depending on the receiving instrument.

The transducer's raw law need not be linear. Where practical, however, the final relationship is easiest to use when it is a known affine law:

$$v_o = a\,x + b\,. \tag{1}$$

Then the indicated physical value is

$$x = \frac{v_o - b}{a}\,. \tag{2}$$

A monotonic nonlinear relationship is still acceptable if it is known and invertible. A non-bijective relationship is unacceptable because one voltage would correspond to several physical values.

Finally, the conditioner must pass the useful signal spectrum and attenuate unwanted spectral components as much as practicable. The frequency-domain model distinguishes a useful spectrum S_u from a disturbance spectrum S_d and motivates a low-pass stage when the disturbance lies at higher frequency.

2.Transducer theory and transfer characteristics

Over the declared measurement range, the transducer law must be invertible. Known zero and span errors can be corrected by calibration; non-correspondence, hysteresis, threshold effects, and dynamic response must be assessed separately.

2.1.The transducer transfer law and why it must be invertible

Let the static forward characteristic be

$$e = f(x), \tag{3}$$

where x is the physical input and e is the electrical output. During measurement, however, the instrument observes e and must infer x. The required operation is therefore

$$x = f^{-1}(e)\,. \tag{4}$$

The inverse exists over the operating range only if the forward law is one-to-one there. For the characteristics considered here, this requires $f(x)$ to be strictly monotonic, either strictly increasing or strictly decreasing, throughout the declared interval.

2.1.1.Why a non-monotonic law fails

A non-monotonic characteristic can cross the same electrical level more than once. In Figure 2, the same reading e_T^* corresponds to x_1, x_2, or x_3; the inverse is therefore ambiguous over that range.

The remedy used here is to restrict operation to a sub-range over which the characteristic is monotonic. The allowable measurement range is therefore part of the transducer specification.

2.1.2.Increasing and decreasing laws are equally valid

A negative slope is not an error. Both increasing and decreasing characteristics are acceptable if they remain monotonic and their inverse law is known. For a small variation, Δe_T and Δx have the same sign for an increasing characteristic and opposite signs for a decreasing characteristic. Therefore, each electrical output in the declared range must correspond to exactly one physical input.

The plot in Figure 2 makes the inversion requirement explicit. The same electrical reading intersects the non-monotonic characteristic at three physical inputs, whereas each strictly monotonic characteristic admits one inverse value over its declared interval.

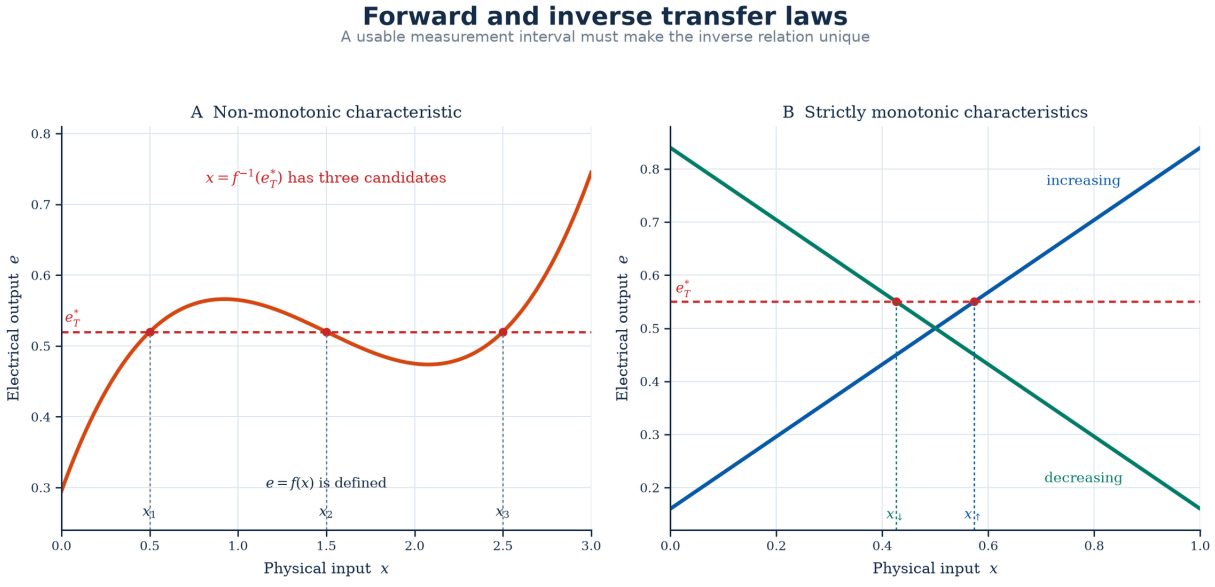


Figure 2. Unique and ambiguous inverse mappings for non-monotonic and monotonic transfer characteristics.

2.2.Linear characteristics, sensitivity, and inverse conversion

The simplest monotonic law is a straight line:

$$e = k\,x + e_0\,. \tag{5}$$

The coefficient k is the slope or static sensitivity:

$$k = \frac{\Delta e}{\Delta x}, \tag{6}$$

and e_0 is the electrical output at $x = 0$. The corresponding inverse is

$$x = \frac{e - e_0}{k}\,. \tag{7}$$

Two points determine the nominal line. If (x_1, e_1) and (x_2, e_2) are known,

$$k = \frac{e_2 - e_1}{x_2 - x_1}, \quad e_0 = e_1 - k\,x_1\,. \tag{8}$$

2.2.1.Dimensional meaning

The slope is not generally dimensionless. Its unit is the output unit divided by the input unit. For a resistance thermometer,

$$[k_R] = \frac{\Omega}{^\circ\mathrm{C}}\,. \tag{9}$$

The intercept has the unit of the output quantity—in this case ohms. Dimensional analysis is useful because it immediately exposes an inverted ratio or an incorrect numerical conversion.

2.2.2.Sensitivity versus resolution

This report distinguishes two concepts that are sometimes both called sensitivity:

- **sensitivity** is the local slope $\mathrm{d}e/\mathrm{d}x$;
- **resolution or threshold** is the smallest input change that produces a detectable output change.

In an ideal continuously responsive device, an arbitrarily small input variation produces a proportional output variation as long as $\mathrm{d}e/\mathrm{d}x$ is non-zero. A real device may instead have a dead interval $\Delta x_{\min}$ within which the output does not change appreciably. In that interval the effective local slope is zero and inputs smaller than the threshold cannot be distinguished.

The plot in Figure 3 separates the ordinate intercept from the useful endpoint span. Sensitivity is the slope between the two declared operating points, and the inverse relation reconstructs the physical input after the offset has been removed.

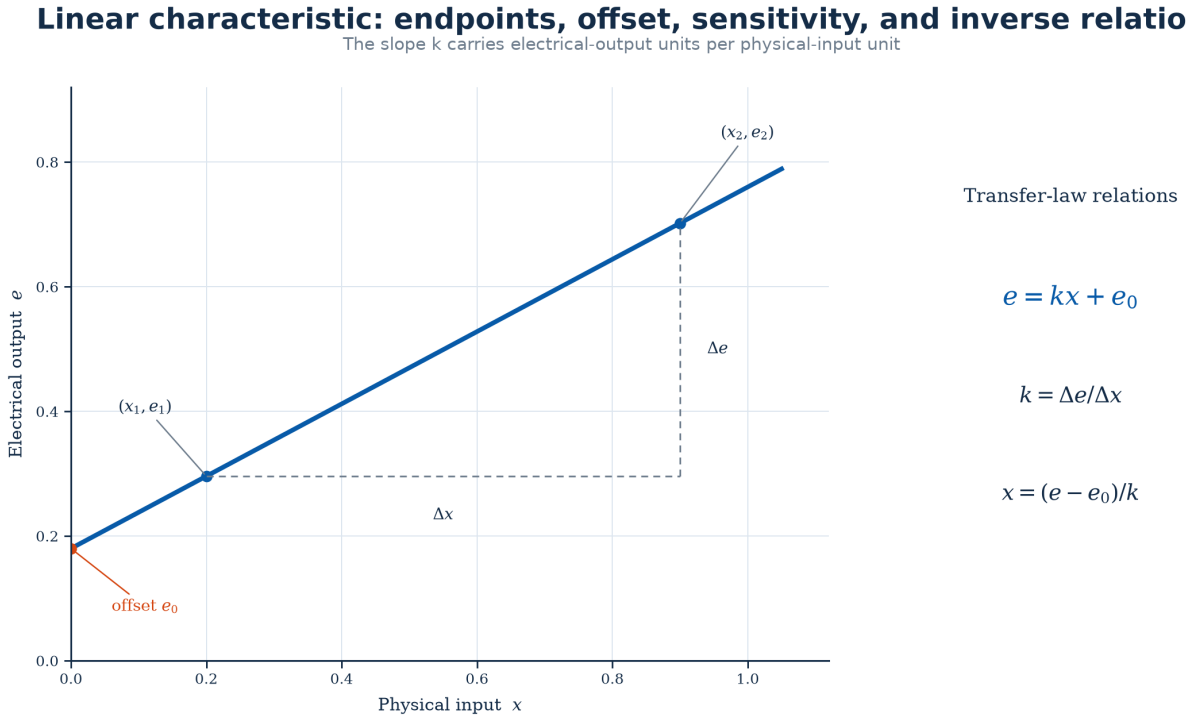


Figure 3. Linear transducer characteristic with offset, endpoint span, sensitivity and inverse relation.

2.3.Real static characteristics and the error taxonomy

An ideal transducer follows its nominal law exactly. A real transducer does not. Three fundamentally different departures from a nominal straight line must be separated.

Let the nominal law be

$$e_{\text{nom}}(x) = k\,x + q\,. \tag{10}$$

A useful decomposition of a real characteristic is

$$e_r(x) = (k + \delta k)x + (q + \delta q) + \delta_{\text{nc}}(x), \tag{11}$$

where:

- δq is the **translation, zero, or offset error**;
- δk is the **coefficient, span, or gain error**;
- $\delta_{\text{nc}}(x)$ is the remaining **non-correspondence** between the actual characteristic and the best corresponding nominal form.

2.3.1.Offset error

If the actual line is parallel to the nominal line but vertically displaced, the error is constant over the input range:

$$\delta q = q_r - q_n\,. \tag{12}$$

For every input, the real electrical output is shifted by the same amount. Once measured, this error can be removed with a summing/subtracting stage or in later digital processing.

The plot in Figure 4 isolates offset error. The actual characteristic remains parallel to the nominal characteristic, so the ordinate displacement is constant throughout the declared input range.

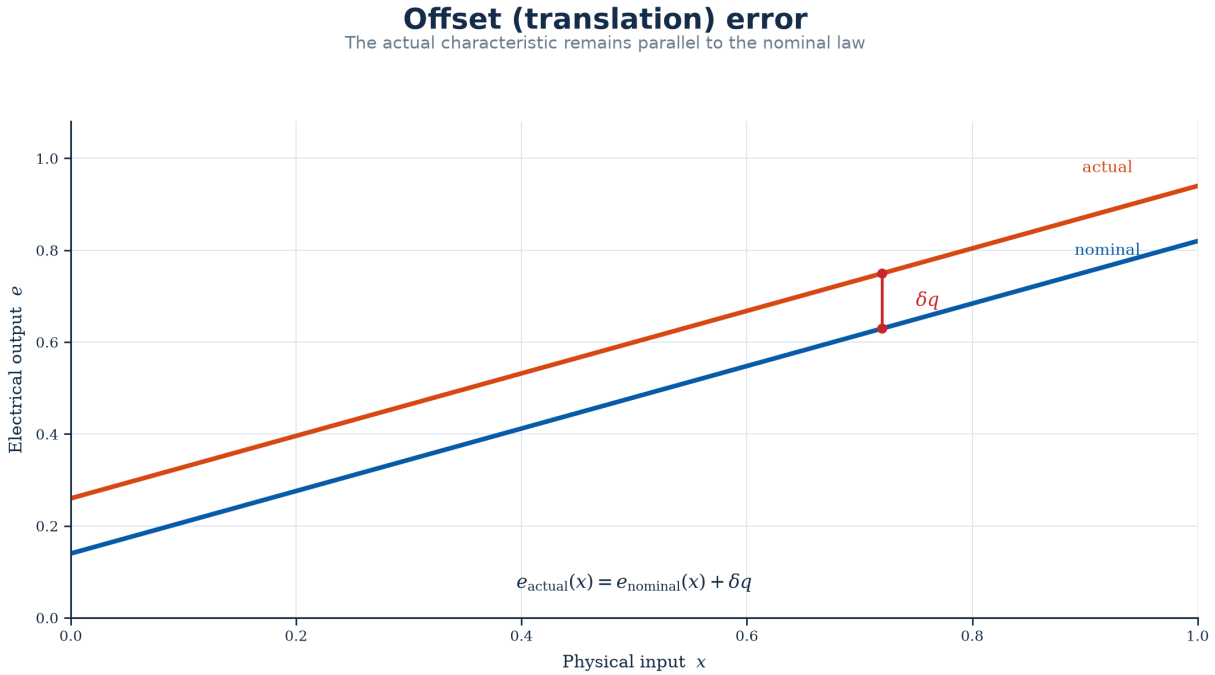


Figure 4. Offset error represented by a constant displacement of the actual characteristic from the nominal characteristic.

2.3.2.Sensitivity or span error

If the real slope differs from the nominal slope, the error varies with input:

$$\delta e_k(x) = \delta k\, x\,. \tag{13}$$

Manufacturers often bound the relative slope error:

$$-\varepsilon_k \le \frac{k_r - k_n}{k_n} \le +\varepsilon_k\,. \tag{14}$$

The Pt100 example takes $k_n = 0.385\,\Omega/°\mathrm{C}$ and a possible real slope between 0.37 and $0.40\,\Omega/°\mathrm{C}$, corresponding approximately to -4% and $+4\%$. Like offset, a known gain error is correctable by multiplication.

The plot in Figure 5 isolates sensitivity error. The nominal and actual characteristics share the same intercept but have different slopes, so their separation grows with input.

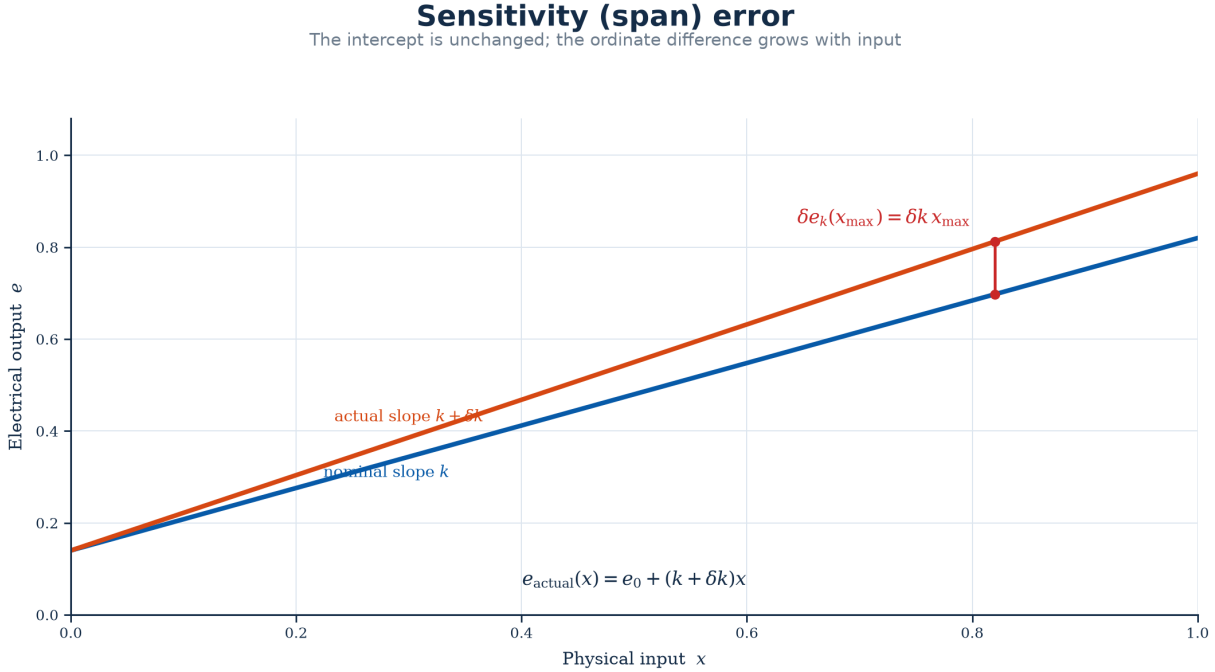


Figure 5. Sensitivity error represented by different slopes of the nominal and actual characteristics.

2.3.3.Non-correspondence and nonlinearity

After removing the best offset and slope correction, the real response may still not coincide with the nominal straight line. This residual is shown as a curved deviation. For a nominal linear characteristic it is conventionally called nonlinearity.

This error is different from offset and gain because it is a function of input rather than one constant. A simple adder and multiplier cannot remove it over the whole range.

The same distinction applies to a transducer whose nominal law is intentionally nonlinear:

$$e_{\text{nom}} = f(x)\,. \tag{15}$$

In that case it is misleading to call the residual “nonlinearity,” because the nominal function is already nonlinear. The correct concept is deviation from the theoretical characteristic:

$$\delta_f(x) = e_r(x) - f(x)\,. \tag{16}$$

Offset-like and gain-like parameter errors may still exist around the nonlinear model, and they may still be correctable if the parameterization is known.

The plot in Figure 6 isolates the residual curvature that remains after zero and span correction. Unlike a constant offset or slope error, this deviation changes with the input and cannot be removed by one additive and one multiplicative correction.

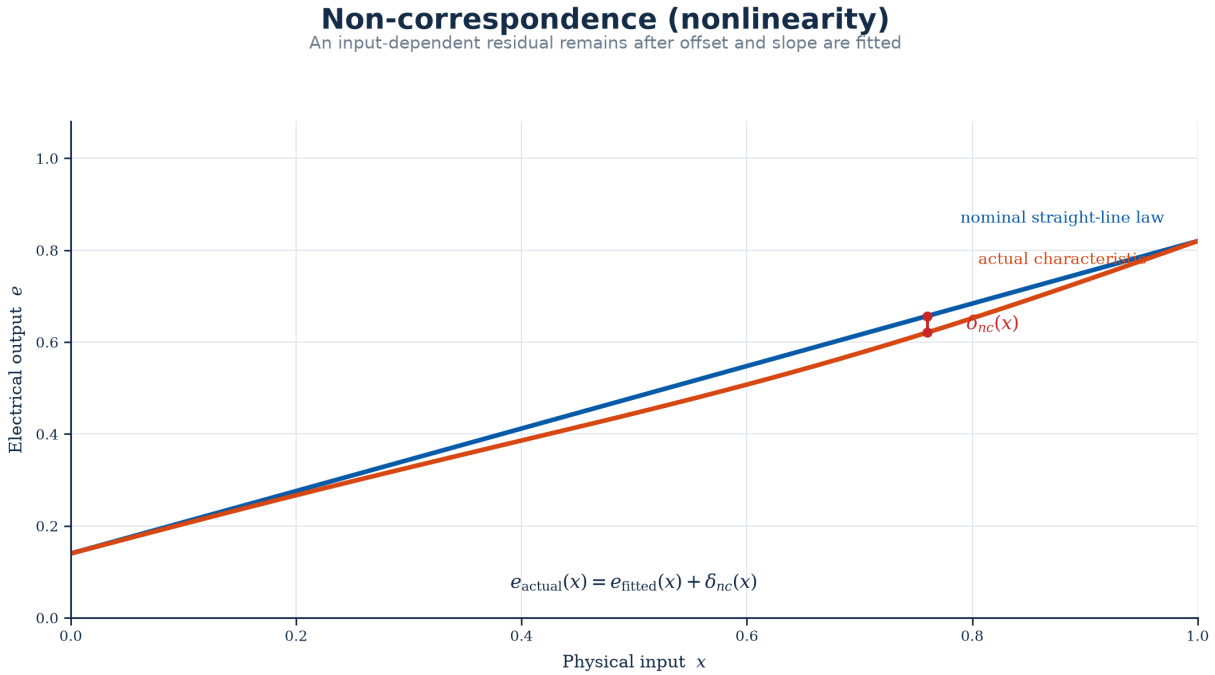


Figure 6. Input-dependent non-correspondence remaining after the best affine correction.

2.3.4.Combined error bands

Offset, slope, and non-correspondence combine into a deterministic tolerance envelope. Offset produces a family of parallel curves, slope variation produces a fan of curves, and residual non-correspondence thickens that fan into an enclosing band. The resulting upper and lower bounds can be written as

$$e_{\text{low}}(x) \leq e_r(x) \leq e_{\text{high}}(x)\,. \tag{17}$$

Given a measured electrical value, this band maps into a possible interval of physical values across the declared range.

The enclosing region is a deterministic error band or tolerance envelope in the input-output graph.

The plot in Figure 7 combines the separate static contributions into a family of possible actual characteristics around the nominal law before calibration. It shows the combined effect of offset, sensitivity error and non-correspondence that the conditioning and calibration stages must accommodate.

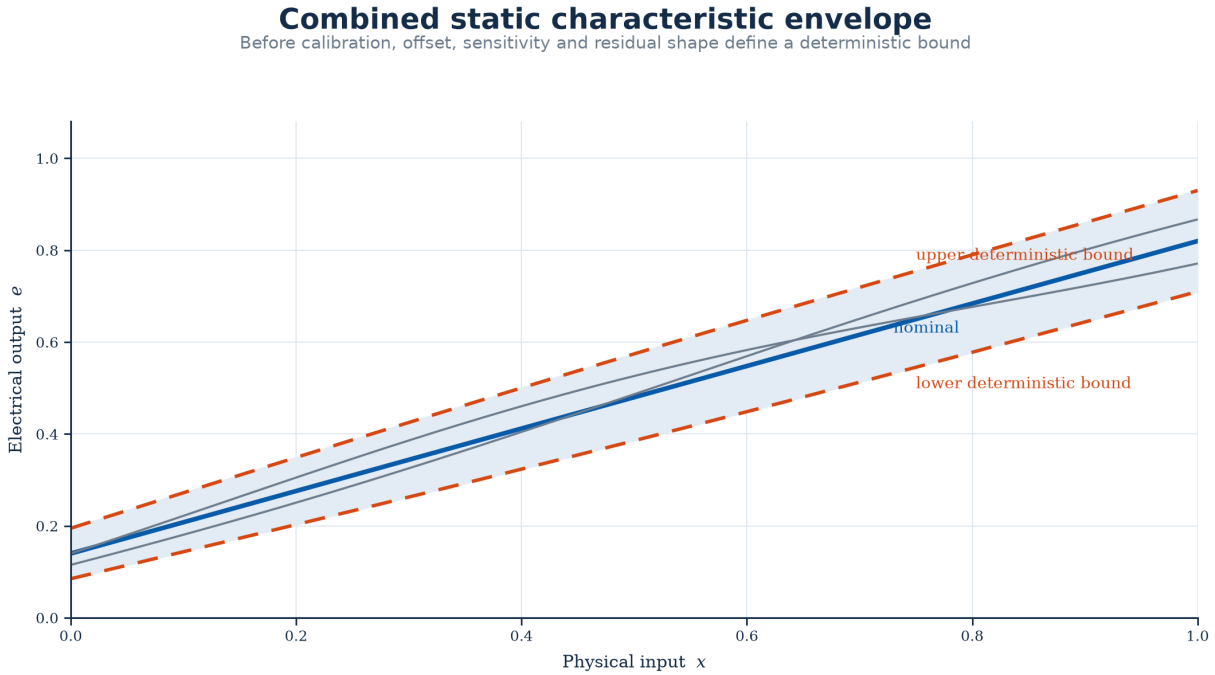


Figure 7. Combined characteristic envelope formed by offset, sensitivity error, and non-correspondence.

2.4.Calibration and what can actually be corrected

A practical calibration hierarchy follows.

2.4.1.Zero calibration

Apply a known reference input x_0, measure the output, and determine the offset discrepancy. For a linear law,

$$\delta q = e_r(x_0) - e_{\text{nom}}(x_0) \tag{18}$$

after any known slope contribution has been accounted for. A subtractor can then remove δq.

2.4.2.Span calibration

Apply two accurately known physical values x_1 and x_2. The measured slope is

$$k_r = \frac{e_r(x_2) - e_r(x_1)}{x_2 - x_1}. \tag{19}$$

The required multiplicative correction is k_n/k_r. Two-point calibration can therefore correct zero and span errors, but it cannot prove linearity between the calibration points.

2.4.3.Multi-point characterization

Non-correspondence is revealed by comparing several points across the operating range rather than only the two endpoints.

2.4.4.Hysteresis cannot be removed by an ordinary static inverse

If the output depends on whether the input approached its present value from above or below, the transducer no longer has a single-valued static characteristic. A correction containing only $e = f(x)$ is insufficient, and a simple offset-and-gain calibration cannot eliminate the hysteresis.

2.5.Hysteresis, threshold, and time-dependent behaviour

2.5.1.Hysteresis

Suppose the input is moved from x_0 to $x_0 + \Delta x$ and then returned to x_0. In an ideal transducer, the output returns to its original value. In a real transducer with hysteresis, the return value differs:

$$e_{\uparrow}(x_0) \neq e_{\downarrow}(x_0)\,. \tag{20}$$

The hysteresis magnitude at a given input may be expressed as

$$h(x) = \left| e_{\uparrow}(x) - e_{\downarrow}(x) \right|. \tag{21}$$

Let $h_{\max}$ be the largest value of $h(x)$ over the declared input range. Relative to the full electrical span $\Delta e_{\mathrm{FS}} = e_{\max} - e_{\min}$,

$$h_{\mathrm{FS}} = \frac{h_{\max}}{\Delta e_{\mathrm{FS}}} \times 100\%\,. \tag{22}$$

A signed directional error may still be defined separately, but its sign depends on the direction of travel. Testing at known points in both directions is therefore required. A small excursion usually produces a small local hysteresis loop, but the relationship need not be analytically simple.

The plot in Figure 8 places the rising and falling branches at the hysteresis discussion: the output at a given input depends on the direction of approach, and their separation is the hysteresis magnitude. The adjoining panel introduces the separate dead-band interval discussed next.

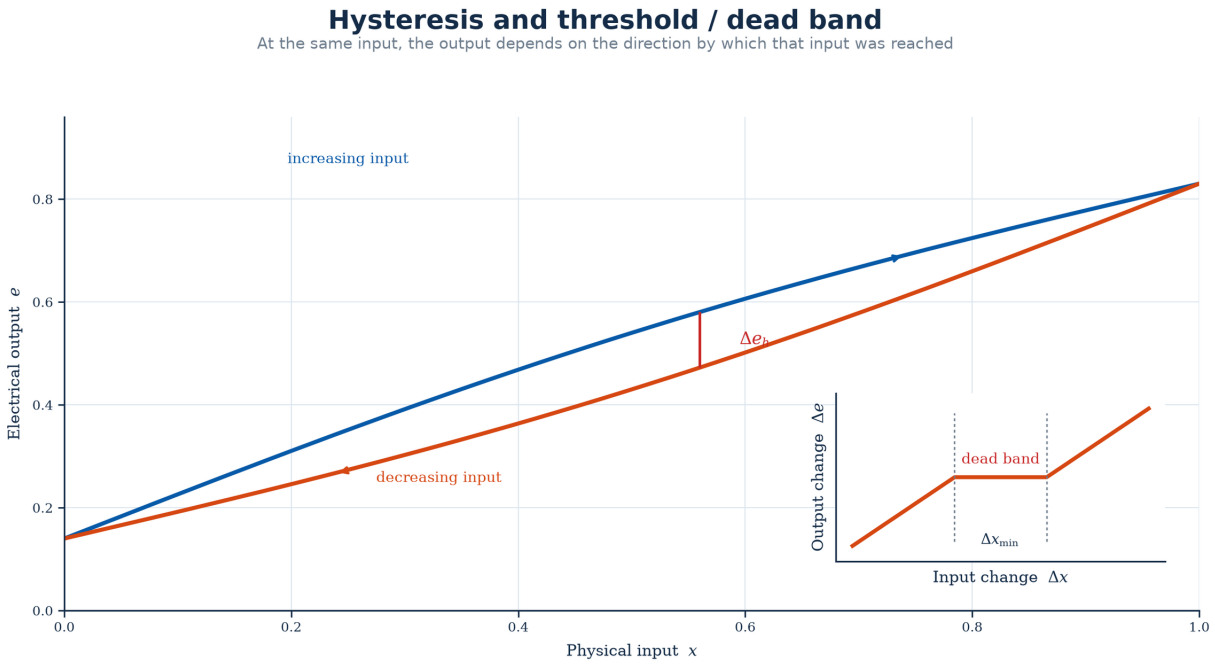


Figure 8. Direction-dependent hysteresis and the distinct local dead-band interval.

2.5.2.Minimum detectable variation and dead band

The threshold is the minimum physical input variation that produces an observable electrical variation. In an ideal device,

$$\lim_{\Delta x \to 0} \left| \frac{\Delta e}{\Delta x} \right| > 0 . \tag{23}$$

In a real device there may be a dead band:

$$|\Delta x| < \Delta x_{\min} \Rightarrow \Delta e \approx 0 . \tag{24}$$

This is a resolution/threshold limitation. It prevents arbitrarily small physical changes from being inferred even when the nominal transfer law is invertible.

2.5.3.Dynamic fidelity

The useful spectral content of the transducer signal must pass through the conditioner so that $v_o(t)$ follows the relevant time evolution of $e_T(t)$. Components outside the useful band may instead be attenuated. The filtering chapter develops this distinction in detail.

3.Mathematical synthesis of the conditioning chain

The required endpoint map determines the overall gain and translation, but a physically valid implementation must also keep every intermediate node within its common-mode, output-swing, noise, and bandwidth limits.

3.1.Why the sensor range should fill the measurement range

Suppose the measurement electronics accepts

$$V_{ADC,min} \leq v_o \leq V_{ADC,max}\,. \tag{25}$$

If the conditioned sensor signal occupies only a small portion of this interval, much of the converter range is unused. The code increment then represents a larger physical increment than necessary. The electrical excursion corresponding to $x_{min}\ldots x_{max}$ should therefore occupy as much of the safe A/D range as possible.

The conditioned sensor interval should use the converter's accepted input range without exceeding it.

If the raw transducer voltage is linear over the selected range, its endpoint form is

$$v_T(x) = v_{T,min} + \frac{v_{T,max} - v_{T,min}}{x_{max} - x_{min}}(x - x_{min})\,. \tag{26}$$

The desired conditioner characteristic is

$$v_o(x) = v_{o,min} + \frac{v_{o,max} - v_{o,min}}{x_{max} - x_{min}}(x - x_{min})\,. \tag{27}$$

Eliminating x gives the required affine electrical transformation:

$$v_o = G v_T + V_0, \tag{28}$$

where

$$G = \frac{\Delta v_o}{\Delta v_T} = \frac{v_{o,max} - v_{o,min}}{v_{T,max} - v_{T,min}}, \tag{29}$$

and

$$V_0 = v_{o,min} - G v_{T,min}\,. \tag{30}$$

These two parameters have distinct meanings. G corrects the span or sensitivity, while V_0 corrects the zero. They implement amplification and translation, respectively.

The corresponding A/D code, assuming a linear converter, is

$$N = N_{min} + \frac{v_o - V_{ADC,min}}{V_{ADC,max} - V_{ADC,min}}(N_{max} - N_{min})\,. \tag{31}$$

The complete physical-to-numerical sensitivity is the product of transducer sensitivity, conditioning gain, and converter codes per volt. This makes clear why every link in the chain must be included in the calibration model.

The plot in Figure 9 aligns the physical, electrical and conditioned intervals on explicit endpoints. The required gain follows from the ratio of output span to input span, while the additive term places the lower endpoint at the required acquisition level.

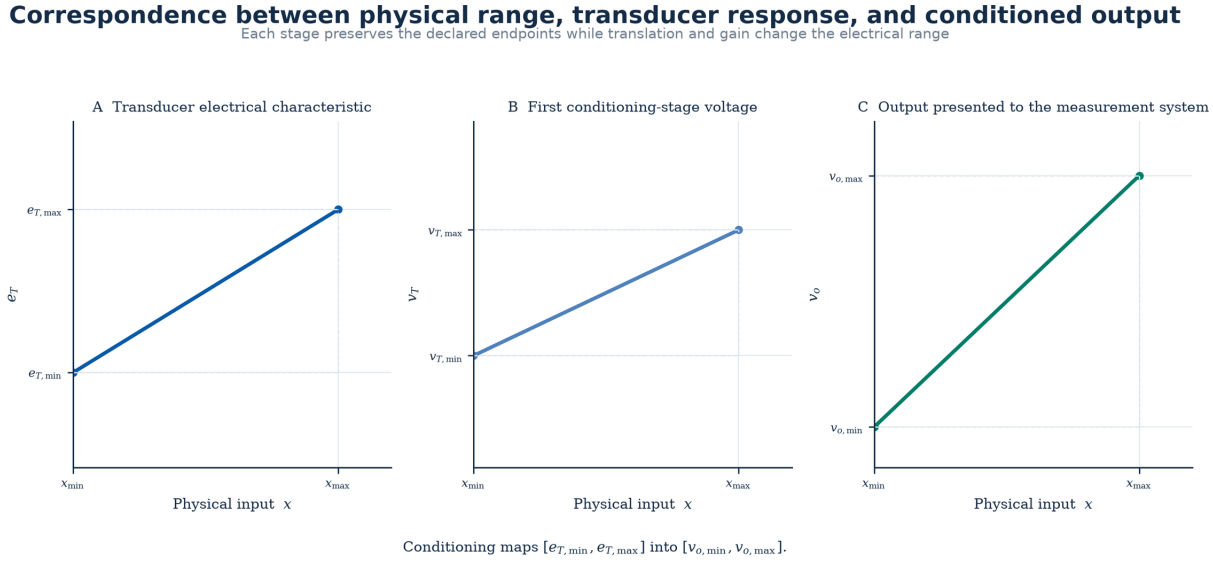


Figure 9. Endpoint mapping from the physical range through the transducer and conditioning stages to the acquisition input.

3.2.Algebraic equivalence versus technological feasibility

Translation and multiplication commute algebraically if the translation value is changed accordingly. For example,

$$G(v_T - a) = Gv_T - Ga\,. \tag{32}$$

Thus one can first subtract a and then amplify by G, or first amplify by G and then subtract Ga. These arrangements are algebraically equivalent at the output but not generally interchangeable in hardware because their intermediate voltages may be completely different.

3.2.1.Order-of-operations headroom check

Consider a sensor that produces 75 to $100\,\mathrm{mV}$ and must be mapped to 0 to $10\,\mathrm{V}$. The required total gain is

$$G_T = \frac{10}{0.100 - 0.075} = 400\,. \tag{33}$$

Subtracting $75\,\mathrm{mV}$ first leaves a 0 to $25\,\mathrm{mV}$ signal, which can then be amplified by 400. Mathematically that is ideal, but generating and preserving a precise $75\,\mathrm{mV}$ analogue reference may be inconvenient.

Amplifying first produces 30 to $40\,\mathrm{V}$, after which a $30\,\mathrm{V}$ translation would be required. That solution is impossible within the assumed internal range of approximately ± 10 to $\pm 12\,\mathrm{V}$. The arithmetic is correct, but the circuit is not realisable with the stated electronics.

3.2.2.Split-gain solution

A split-gain architecture resolves the headroom problem:

$$v_x = G_1 v_T, \tag{34}$$

$$v_y = v_x + E_0, \tag{35}$$

$$v_o = G_2 v_y, \tag{36}$$

so that

$$G_T = G_1 G_2 . \tag{37}$$

The first gain is selected to use the internal voltage range without saturating it. The translation is selected from a small set of accurate, stable references. The second gain supplies the remainder. For a required zero output at $v_{T,min}$,

$$E_0 = - G_1 v_{T,min}, \tag{38}$$

and therefore

$$G_2 = \frac{G_T}{G_1} . \tag{39}$$

If the desired lower output is not zero, the more general relation is

$$E_0 = \frac{v_{o,min}}{G_2} - G_1 v_{T,min} . \tag{40}$$

The split is constrained by every internal node, not only by the final output:

$$| G_1 v_T | \leq V_{int,max}, \tag{41}$$

$$| G_1 v_T + E_0 | \leq V_{int,max}, \tag{42}$$

$$v_{o,min,allowed} \leq G_2 (G_1 v_T + E_0) \leq v_{o,max,allowed} . \tag{43}$$

The operational amplifiers' input common-mode ranges, output swing under load, and reference-pin range must also be checked. The worked examples use about $10\,\mathrm{V}$ as a convenient internal maximum and reference values around 1.25, 2.5, 5, 7.5, and $10\,\mathrm{V}$, with 2.5 and $5\,\mathrm{V}$ as the most readily available. These are design examples, not universal limits.

The circuit in Figure 10 implements the split-gain solution as a sequence of moderate gain, reference translation and further gain. The final affine law is unchanged, but the reference is inserted at a node where its magnitude and the signal common level remain compatible with the available supply rails.

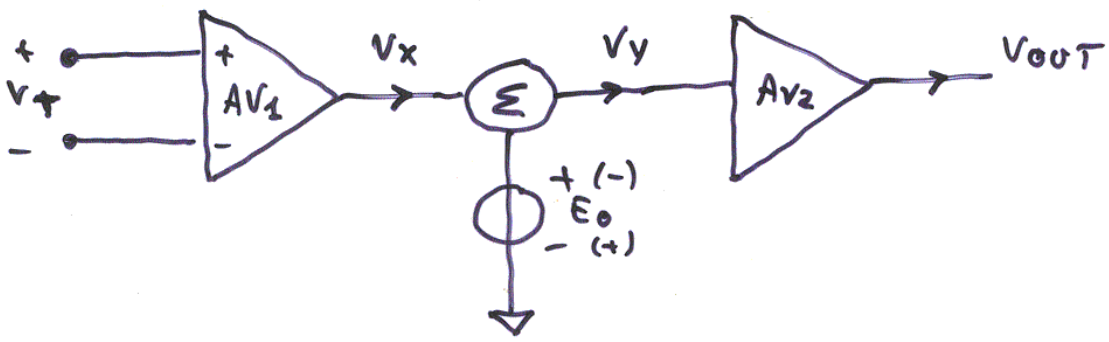


Figure 10. Two-stage gain and reference chain used to keep intermediate voltages within bounds.

3.2.3.Worked split-gain mapping

For the 75 to $100\,\mathrm{mV}$ example, choosing $E_0 = -5\,\mathrm{V}$ gives

$$G_1 = \frac{5}{0.075} = 66.67, \tag{44}$$

$$v_x = 5.00\ldots6.67\,\mathrm{V}, \tag{45}$$

$$v_y = 0\ldots1.67\,\mathrm{V}, \tag{46}$$

and

$$G_2 = \frac{400}{66.67} = 6\,. \tag{47}$$

Every internal node remains in the assumed range and the final output is 0 to $10\,\mathrm{V}$. The result demonstrates the required combination of endpoint mapping and internal-node feasibility.

The plot in Figure 11 plots the selected intermediate ranges for the successful ordering. The first gain raises the sensor span to a manageable level, translation removes the unwanted common level, and the second gain expands the bounded result to the required output span without exceeding the internal-node limits.

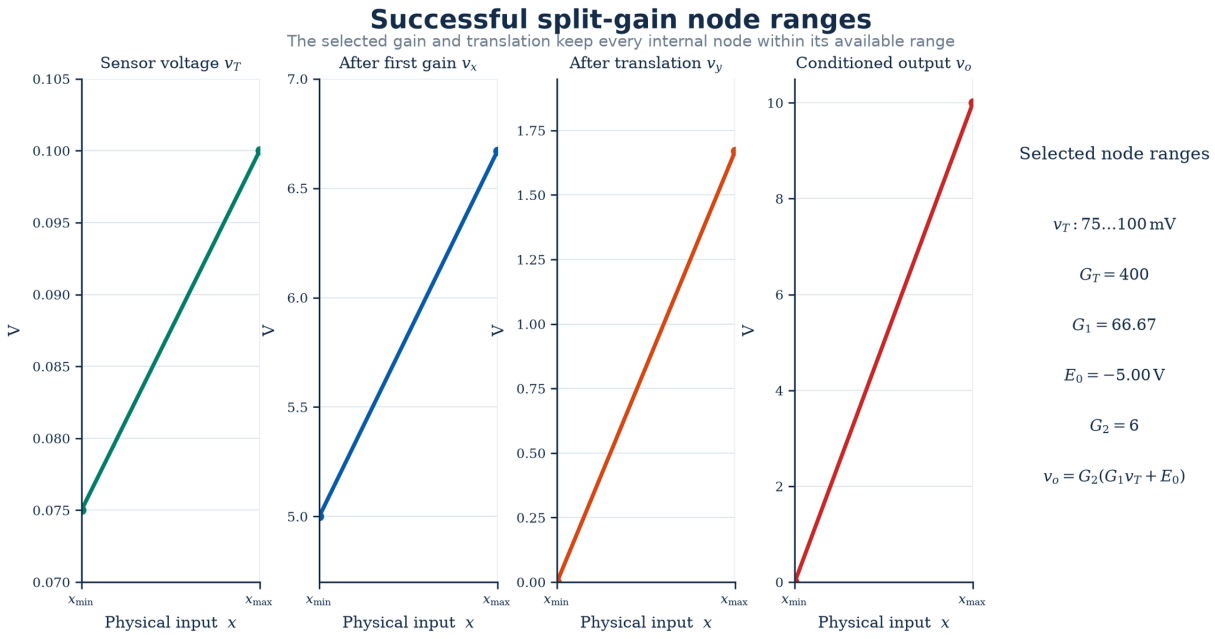


Figure 11. Successful split-gain mapping with the voltage range shown at every internal node.

4.Electrical output domains, excitation, and loading

The electrical interface must be chosen from the sensor's actual output domain and must not disturb the measurand or the transducer characteristic it is intended to observe.

4.1.The Pt100 measurement chain: from resistance to a usable signal

The Pt100 exposes the complete measurement problem in one example. Temperature first changes the sensor resistance; controlled excitation converts that resistance into a voltage; the connection topology determines whether the voltage belongs to the sensor alone or also contains lead drops; and the conditioning electronics translates and amplifies the sensed millivolt range into a signal accepted by the receiving instrument.

4.1.1.Nominal resistance-temperature law

The worked example uses the linearised relation

$$R(T) = R_0 + k_R T, \tag{48}$$

with

$$R_0 = 100\ \Omega, \quad k_R = 0.385\ \Omega/^\circ\mathrm{C}\,. \tag{49}$$

Over the selected interval,

$$R(-50^\circ\mathrm{C}) = 80.75\ \Omega, \quad R(100^\circ\mathrm{C}) = 138.5\ \Omega, \tag{50}$$

and therefore

$$\Delta R = 57.75\ \Omega\,. \tag{51}$$

The underlying physical idea is that the resistivity of the platinum conductor changes with temperature. For a uniform conductor,

$$R = \rho \frac{\ell}{S}, \tag{52}$$

where ρ is resistivity, ℓ is conductor length, and S is cross-sectional area. The linearised Pt100 law is the nominal model used to relate that material behaviour to temperature over the stated interval.

The plot in Figure 12 gives the resistance law used in the Pt100 example. The marked values identify the nominal 100-ohm resistance at 0 degrees Celsius, the positive temperature coefficient, and the resistance endpoints associated with the stated temperature interval.

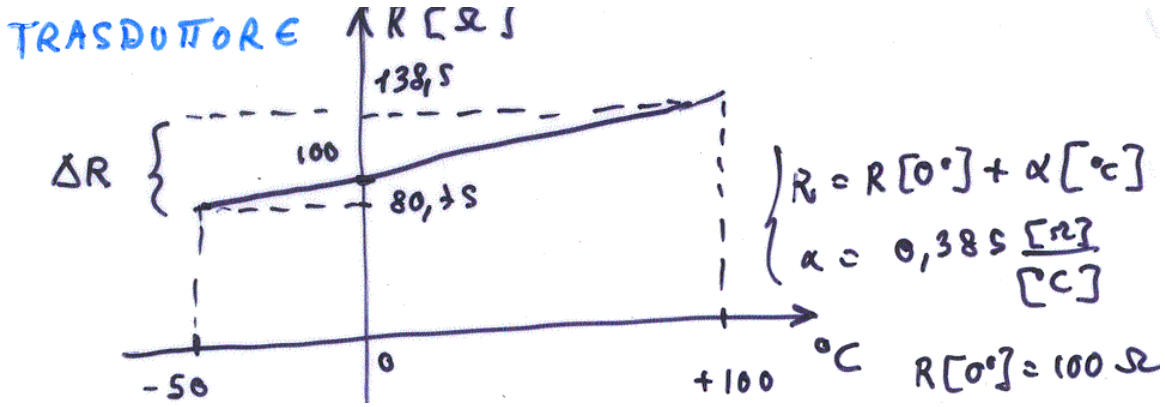


Figure 12. Pt100 resistance-temperature characteristic over the stated operating interval.

4.1.2.Current excitation converts resistance into a voltage

Resistance is information, but it is not yet a transportable signal for a voltage-input instrument. A controlled current converts the resistance into a voltage while preserving its dependence on temperature:

$$V_x = I_{\text{exc}} R_x \,. \tag{53}$$

For $I_{\text{exc}} = 1\,\text{mA}$,

$$V_x(T) = 10^{-3} R(T) = 0.100 + 0.000385T\ [\text{V}], \tag{54}$$

so the electrical sensitivity is

$$\frac{dV_x}{dT} = 0.385\ \text{mV/°C}\,. \tag{55}$$

The selected temperature interval therefore becomes a voltage interval from $80.75\,\text{mV}$ at $-50\,°\text{C}$ to $138.5\,\text{mV}$ at $100\,°\text{C}$.

4.1.3.The connection must preserve the sensor voltage

The running example assumes a four-wire connection. Two force conductors carry the excitation current, while two separate high-impedance sense conductors present the voltage directly across the Pt100 to a differential receiver. Under the ideal high-input-resistance assumption,

$$V_{\text{sense}} = I_{\text{exc}} R(T)\,. \tag{56}$$

The voltage drops in the force leads then consume excitation compliance but do not enter the measured differential voltage. If the same two conductors carry both current and sensed voltage, the measured quantity instead contains the two lead resistances. The two- and four-wire cases are derived separately after the end-to-end chain has been established.

4.1.4.Translation and gain produce the usable output signal

The sensed voltage is now a valid representation of temperature, but its $57.75\,\text{mV}$ span is still too small and it carries a $100\,\text{mV}$ value at $0\,°\text{C}$. For the stated -50 to $+100\,°\text{C}$ interval, the worked target is -5 to $+10\,\text{V}$. Removing the $0\,°\text{C}$ baseline and applying the endpoint gain gives

$$V_{\text{out}} = G\left(V_{\text{sense}} - 0.100\right), \tag{57}$$

where

$$G = \frac{10 - (-5)}{0.1385 - 0.08075} = 259.74\,. \tag{58}$$

Substitution of the Pt100 voltage law yields

$$V_{\text{out}} = 0.1T\ [\text{V}]\,. \tag{59}$$

The complete measurement relation is therefore

$$T \rightarrow R(T) \rightarrow V_{\text{sense}} = I_{\text{exc}} R(T) \rightarrow V_{\text{out}} = 259.74\left(V_{\text{sense}} - 0.100\right)\,. \tag{60}$$

At $-50\,°\text{C}$ the output is $-5\,\text{V}$, at $0\,°\text{C}$ it is $0\,\text{V}$, and at $100\,°\text{C}$ it is $10\,\text{V}$. The receiving system can recover temperature directly from

$$T[°\text{C}] = 10V_{\text{out}}[\text{V}]\,. \tag{61}$$

This establishes the complete ideal channel before the practical limitations of its excitation source, wiring and receiver are examined. The later gain-and-calibration chapter determines how the translation and total gain are distributed among real stages without exceeding their internal voltage ranges.

4.1.5.Excitation current and self-heating

The excitation current cannot simply be made arbitrarily large to increase signal amplitude. The Pt100 dissipates

$$P = I_{\text{exc}}^2 R_x, \tag{62}$$

and that power heats the sensing element. Because the sensor is intended to measure the surrounding temperature, this self-heating changes the measurand at the sensor and therefore introduces a systematic error.

Two requirements oppose one another:

- electrically, a larger current produces a larger and easier-to-measure voltage;
- physically, a smaller current reduces self-heating and perturbation of the temperature being measured.

The examples use approximately 0.5 to $2\,\text{mA}$, with $1\,\text{mA}$ as the worked value. The excitation current must remain low enough that self-heating does not significantly alter the measured temperature.

4.2.Practical current excitation for the Pt100

A precision current sink for Pt100-class sensors can use a stable reference, for example $5\,\text{V}$ from a REF02-type device, an operational amplifier, and an N-channel MOSFET such as a 2N7000 or BS170. The feedback loop forces the sense-resistor voltage to equal the reference input:

$$I_S = \frac{V_{ref}}{R_{sh}}. \tag{63}$$

Because MOSFET gate current is ideally negligible,

$$I_D \simeq I_S, \tag{64}$$

so the sensor current at the drain is

$$J \simeq \frac{V_{ref}}{R_{sh}}. \tag{65}$$

An illustrative combination is $V_{ref} = 5\,\text{V}$ and $R_{sh} = 10\,\text{k}\Omega$, which yields $0.5\,\text{mA}$. The circuit is a sink rather than a source: current flows through the remote sensor into the MOSFET drain and through the sense resistor toward the negative supply.

The ideal relation requires sufficient compliance voltage across the sensor, wiring, MOSFET, and sense resistor.

The circuit in Figure 13 shows that a constant excitation current converts the resistance characteristic into a voltage characteristic. Increasing current increases the resulting voltage excursion and electrical sensitivity, but it also increases sensor dissipation.

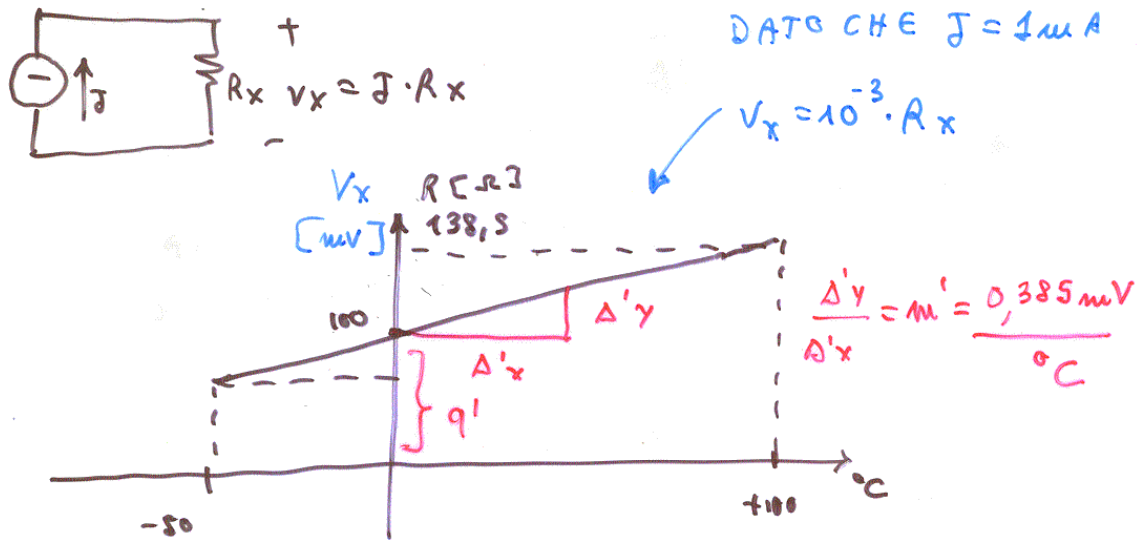


Figure 13. Constant-current excitation of a Pt100 and the resulting voltage sensitivity.

4.3.Lead resistance and remote Pt100 connections

The Kelvin connection follows directly from separating the force-current path from the voltage-sensing path.

4.3.1.Two-wire measurement

If the same pair of wires carries excitation current and returns the measured voltage, the voltmeter sees the sensor and both lead resistances:

$$v_m = J(R_x + R_{f+} + R_{f-}) . \tag{66}$$

For equal leads,

$$v_m = J(R_x + 2R_f) . \tag{67}$$

Interpreting this voltage as JR_x produces an absolute resistance error of $2R_f$ and an approximate relative error

$$\varepsilon_R \simeq \frac{2R_f}{R_x} . \tag{68}$$

The arrangement is acceptable only when $R_x \gg R_f$. This is why ordinary two-lead ohmmeters are adequate for hundreds of ohms or more but poor for small changes around a low nominal resistance.

The conductor resistance is

$$R_f = \rho \frac{\ell}{S}, \tag{69}$$

where ρ is resistivity, ℓ is lead length, and S is cross-sectional area. A representative copper resistivity is approximately $0.017\,\Omega\,\mathrm{mm}^2/\mathrm{m}$. Longer and thinner wires increase the error; merely knowing that a cable is copper does not make its resistance negligible.

The circuit in Figure 14 shows the two-wire error mechanism directly. The excitation current crosses both lead resistances before returning from the sensor, so the measured voltage contains the sensor drop plus two lead-resistance drops.

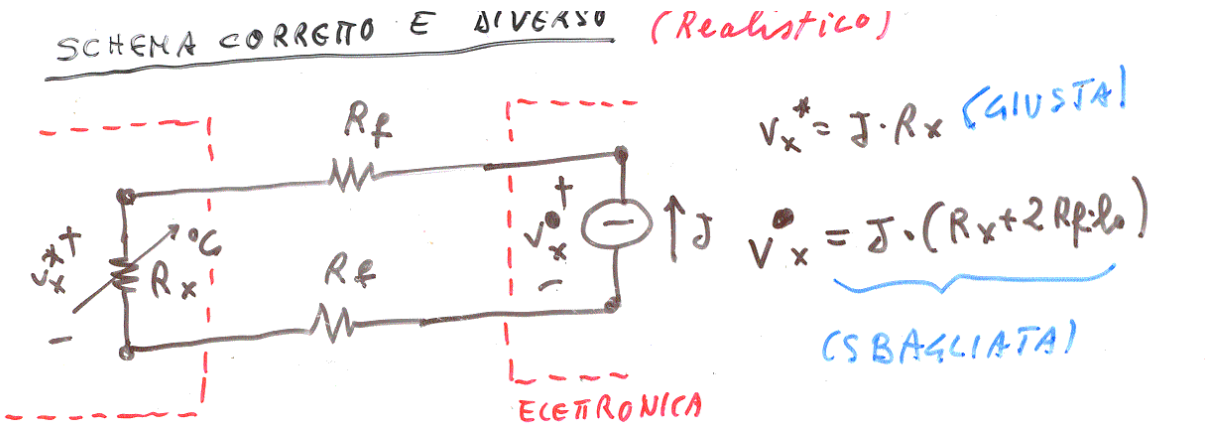


Figure 14. Two-wire resistance measurement including both lead resistances in the measured voltage.

4.3.2.Ideal four-wire measurement

The four-wire arrangement separates the two functions:

- two **force** leads carry the excitation current through R_x;
- two **sense** leads connect a differential, very-high-input-resistance voltmeter directly to the sensor terminals.

With an ideal voltmeter, $R_V \to \infty$, sense current is zero. The force-lead voltage drops affect the compliance required from the current source but do not appear in the sensed voltage:

$$v_m = v_x = JR_x\,. \tag{70}$$

The sense receiver must be differential because neither remote sensor terminal is guaranteed to be at the instrument's ground potential. It must also have very high and reasonably balanced input impedance. A single-ended voltmeter referred to ground does not preserve the ideal four-wire argument.

The circuit in Figure 15 separates the force loop from the voltage-sensing loop. Because the sensing input draws negligible current, the receiver observes the voltage across the resistive element rather than the voltage across the force wiring.

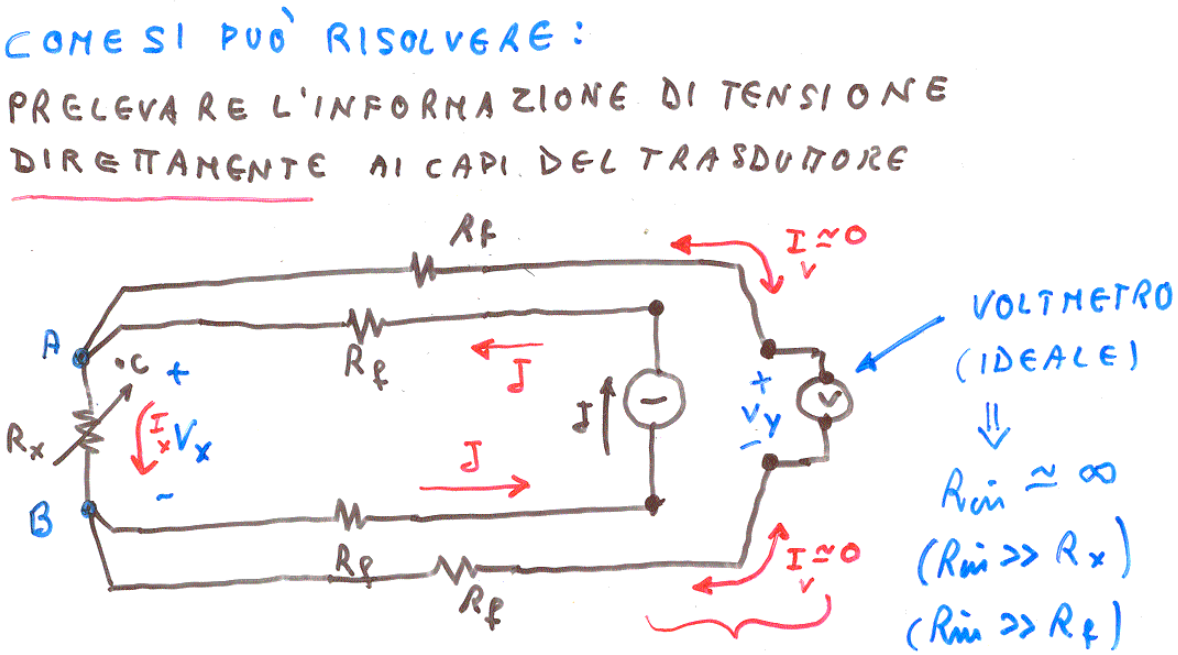


Figure 15. Four-wire Kelvin connection with separate excitation and high-impedance sensing conductors.

4.3.3.Error with a real voltmeter

When the assumption $R_V = \infty$ is removed, the sense branch, consisting of two sense-lead resistances and the voltmeter input resistance, draws a current I'. For equal sense leads,

$$I' = \frac{v_x}{R_V + 2R_f}. \tag{71}$$

The excitation current splits, so the sensor current is

$$I_x = J - I'. \tag{72}$$

Solving the two relations gives

$$I' = \frac{JR_x}{R_x + R_V + 2R_f}, \tag{73}$$

and the voltage actually indicated across R_V is

$$v_m = I'R_V = JR_x \frac{R_V}{R_x + R_V + 2R_f}. \tag{74}$$

For $R_V \gg R_x + 2R_f$,

$$\frac{v_m - JR_x}{JR_x} \simeq -\frac{R_x + 2R_f}{R_V}. \tag{75}$$

This derivation explains both residual mechanisms: the sense branch diverts some of the source current away from the sensor, and its own lead resistances drop part of the voltage before it reaches the receiver. The error becomes small, not identically zero, when the receiver input resistance is merely finite and large.

The circuit in Figure 16 adds the finite input resistance omitted by the ideal construction. A small sense current then flows and produces residual error through the sense leads; the error becomes negligible only when the receiver resistance is sufficiently large relative to the complete sense path.

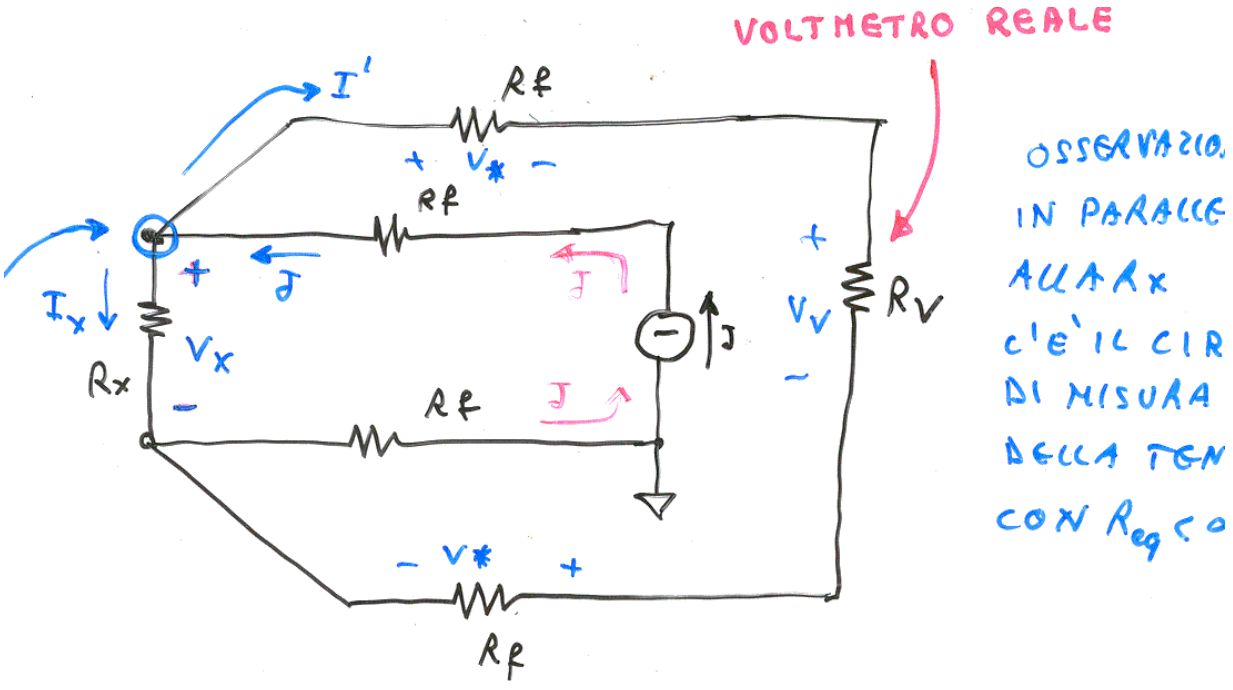


Figure 16. Four-wire Kelvin circuit including finite receiver input resistance.

4.3.4.Do not confuse two different meanings of “four wire”

A bridge-transducer connection may also use four wires: two excite the bridge and two carry its differential output. This is not the same topology as a four-wire Kelvin resistance measurement. A bridge with remote excitation sensing generally needs two additional sense conductors, giving a six-wire transducer connection. The two arrangements must be named explicitly so that “four wire” does not conceal different functions.

4.4.Differential reception of the remote sensor voltage

The four-wire method naturally leads to a differential input stage because the desired voltage is the difference between two remote nodes, neither of which should be assumed equal to ground.

Let the two input voltages relative to an arbitrary reference be V_A and V_B. Define

$$V_D = V_A - V_B \tag{76}$$

and

$$V_C = \frac{V_A + V_B}{2}. \tag{77}$$

The two node voltages can then be reconstructed as

$$V_A = V_C + \frac{V_D}{2}, \quad V_B = V_C - \frac{V_D}{2}. \tag{78}$$

V_D is the differential signal containing the desired measurement. V_C is the common-mode level shared by the two inputs relative to the reference node.

4.4.1.Ideal differential amplifier

An ideal differential amplifier responds only to the difference:

$$V_o = A_D(V_A - V_B) = A_D V_D. \tag{79}$$

It is insensitive to V_C. The three examples on the final page demonstrate this directly:

- common-mode input only: $V_D = 0$, so $V_{\text{out}} = 0$, regardless of the sign or magnitude of V_C within the amplifier's valid input range;
- differential input only: $V_{\text{out}} = A_D V_D$;
- common-mode plus differential input: the output remains $A_D V_D$.

In a real amplifier one may write

$$V_o = A_D V_D + A_C V_C, \tag{80}$$

where A_C is the residual common-mode gain. The ideal model sets $A_C = 0$; a component-level design must additionally specify common-mode input range and common-mode rejection ratio.

4.4.2.Why this matters in a remote sensor cable

Interference induced similarly on both sense wires appears mainly as common-mode voltage. A differential front end rejects that shared component while amplifying the small voltage difference created by the sensor. High input resistance simultaneously ensures that the sense conductors carry negligible current and therefore develop negligible resistive drop.

The first amplification stage must therefore be differential and high impedance. This is not merely an amplifier preference; it is part of the measurement topology.

The diagram in Figure 17 represents the common-mode-only case. The two input nodes are driven by the same voltage relative to the reference, so their difference is zero and an ideal differential amplifier produces zero output even though both absolute input voltages may be large.

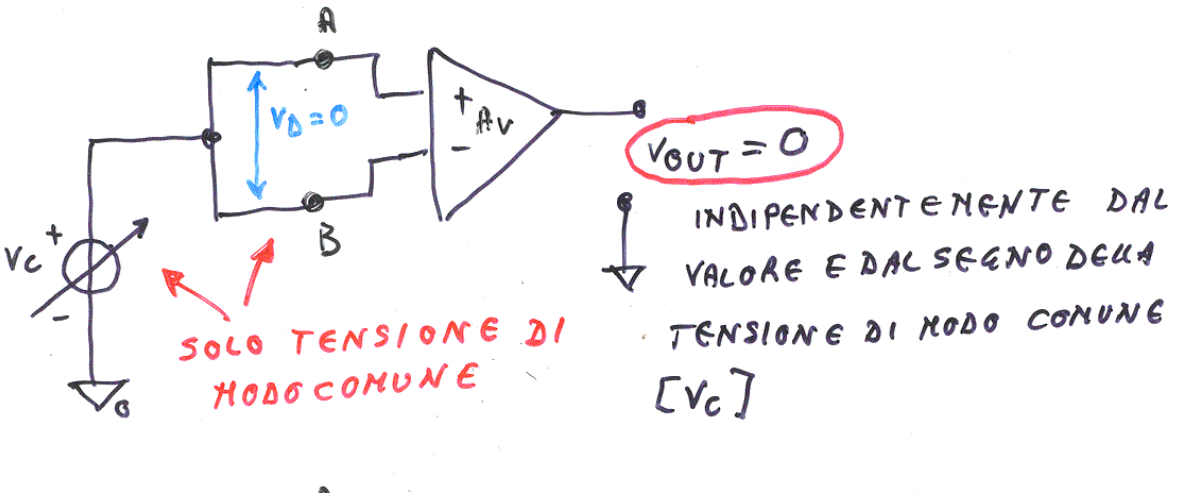


Figure 17. Common-mode limiting case with equal voltages at the two differential inputs.

The diagram in Figure 18 represents the differential-only case. Equal and opposite voltages place the input midpoint at the reference potential while preserving their separation; the output therefore equals the differential input multiplied by the differential gain.

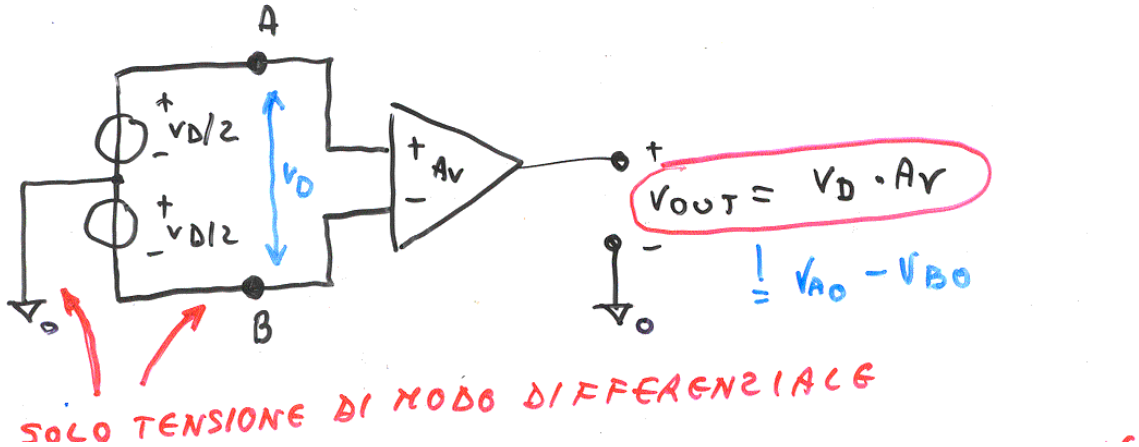


Figure 18. Differential-only limiting case with equal and opposite input voltages.

The diagram in Figure 19 combines the two components. The same common-mode voltage is added to both conductors while equal and opposite half-differential voltages establish their separation; an ideal stage responds to the separation and rejects the shared displacement.

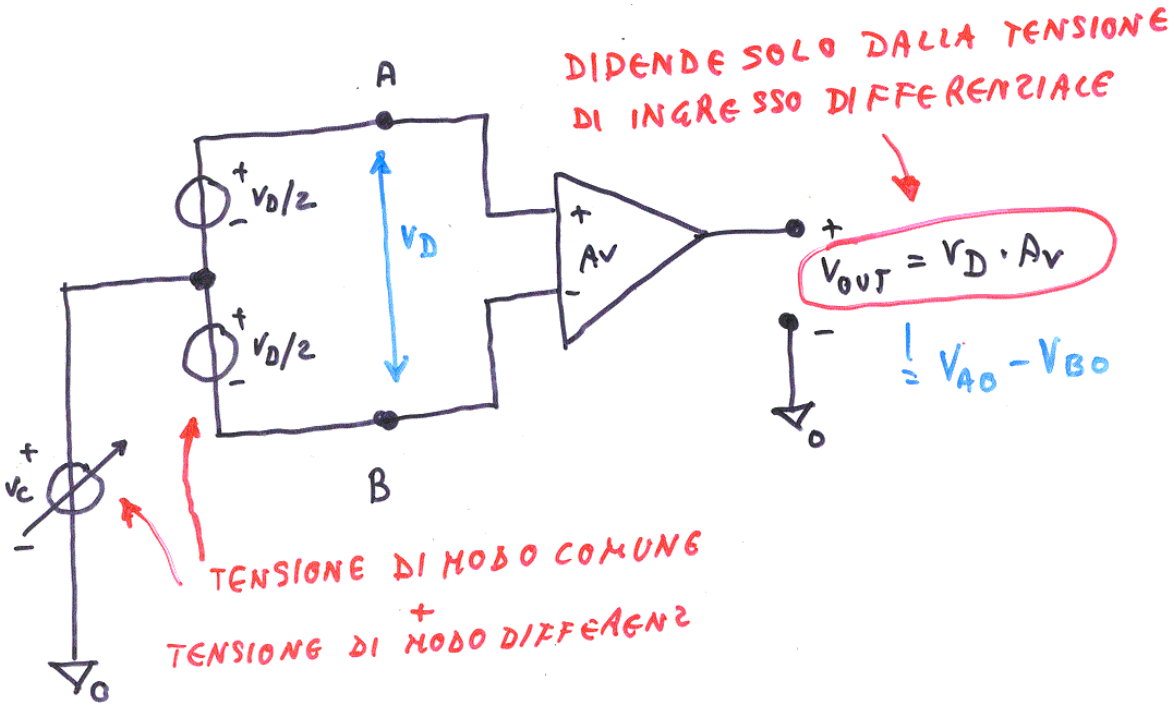


Figure 19. Combined common-mode and differential excitation of a differential amplifier.

4.5.Other sensor domains and input conversions

Once the resistive-sensor chain has been completed, the remaining interfaces can be introduced by the electrical quantity they must convert. Voltage-excited bridges require regulated excitation, existing voltage sources require an appropriate input impedance, current-output devices require current-to-voltage conversion, and piezoelectric sensors require charge conversion.

4.5.1.Sensor excitation by regulated voltage and remote sense

Bridge sensors, such as load cells, are normally excited by a stable voltage, often 5 or $10\,\mathrm{V}$ in the worked examples. Because their output is proportional both to the measurand and to excitation voltage,

$$v_T = k_x x\, V_{exc}, \tag{81}$$

excitation error is directly a sensitivity error unless the measurement is made ratiometrically.

A remote-sense voltage regulator takes feedback from the load terminals through a differential network formed by equal resistor ratios. If the resistor ratios are matched, the sense inputs draw negligible current, the force lead resistance is small relative to the feedback resistances, and the power stage retains compliance, the loop makes the remote load voltage approximately equal to the programmed input:

$$V_{load} \simeq V_{set}\,. \tag{82}$$

The force outputs automatically rise or fall enough to compensate their lead drops. A shunt resistor can provide load-current information. An enhanced version adds a pass transistor both to increase available output current and to enforce a limit, with

$$I_{max} \simeq \frac{0.6\,\mathrm{V}}{R_{sh}}, \tag{83}$$

which corresponds to a bipolar transistor's base-emitter threshold in such a limiter. The exact limit varies with device, temperature, and topology and should not be treated as a precision equation.

Remote sensing compensates the steady voltage drop in the force leads by taking feedback from the remote load terminals.

4.5.2.Single-ended voltage input

For a laboratory source or a signal already referred to the conditioner ground, a single-ended input may use a defined resistance of several kilohms or $50\,\Omega$. Because common mode denotes the component shared by two differential inputs, this topology is designated a **single-ended, ground-referenced voltage input**.

Input resistance is selected according to source expectations. A $50\,\Omega$ termination is appropriate only for a source and cable system intended to drive it. It would seriously load many sensors.

4.5.3.Current-to-voltage conversion

For a current-output transducer, the input op amp is used as a transimpedance amplifier. Its summing node is held near a virtual reference, so the effective input resistance is approximately zero. With feedback resistance R_F,

$$v_o = V_{REF} - I_{in}R_F, \tag{84}$$

where the sign depends on current direction. Changing R_F changes the current-to-voltage conversion factor.

For a photodiode, shifting the summing-node reference imposes the bias shown in the input-stage arrangement.

A 4 to $20\,\mathrm{mA}$ industrial transmitter can be read with the same principle or with a precision shunt followed by a voltage amplifier. Its $4\,\mathrm{mA}$ lower endpoint is a live zero, not physical zero; the subsequent affine mapping must subtract that baseline before scaling to the converter range.

Figure 20 recalls the complementary resistance-to-voltage case: the conditioning circuit imposes a constant current, while the sensor resistance varies with the measurand. The measured voltage is $v_x = JR_x$. In a current-output interface, the sensor instead supplies the variable current and the conversion resistance is fixed.

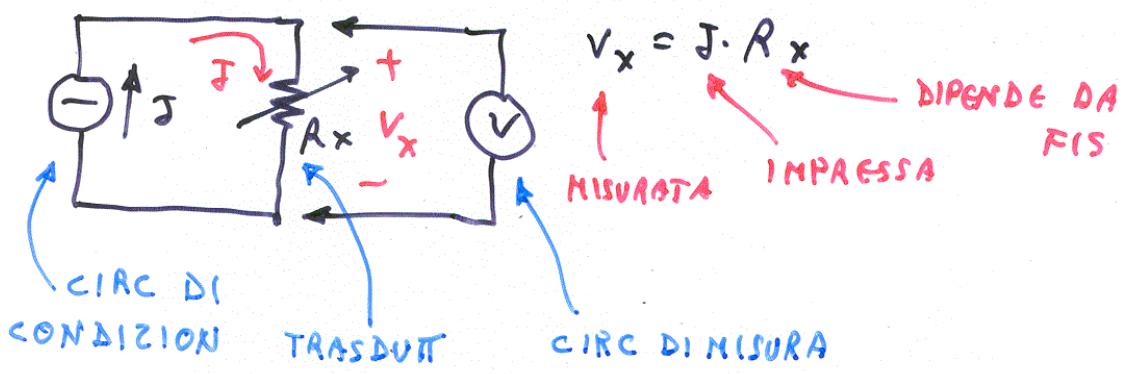


Figure 20. Resistance-output transducer measured as a voltage under constant-current excitation.

4.5.4.Charge amplification

Piezoelectric sensors generate charge rather than a stable DC voltage. A charge amplifier uses a feedback capacitor C_F so that

$$\Delta v_o = -\frac{\Delta Q}{C_F}. \tag{85}$$

Selecting C_F selects the charge sensitivity. A large resistor R_F in parallel with the capacitor provides a DC return path and prevents the op amp from integrating bias and leakage current until it saturates. It creates the lower cutoff

$$f_L = \frac{1}{2\pi R_F C_F}. \tag{86}$$

The illustrated feedback resistance is approximately $20\,\mathrm{M\Omega}$. A FET-input operational amplifier provides the high input impedance required by the charge-amplifier stage.

5.Analogue input integrity and interference control

Interference must be controlled according to its coupling path before a large out-of-band or common-mode signal drives the front end into a nonlinear region.

5.1.The analogue input as an electrical interconnection

An analogue signal cannot be considered independently of the circuit that produces it and the circuit that receives it. The source is usefully represented by its Thevenin equivalent: an ideal voltage generator $v_i(t)$ in series with a source resistance R_{si}. The receiving electronics presents an input resistance R_{IN}.

The loaded source-and-receiver boundary is shown in Figure 21.

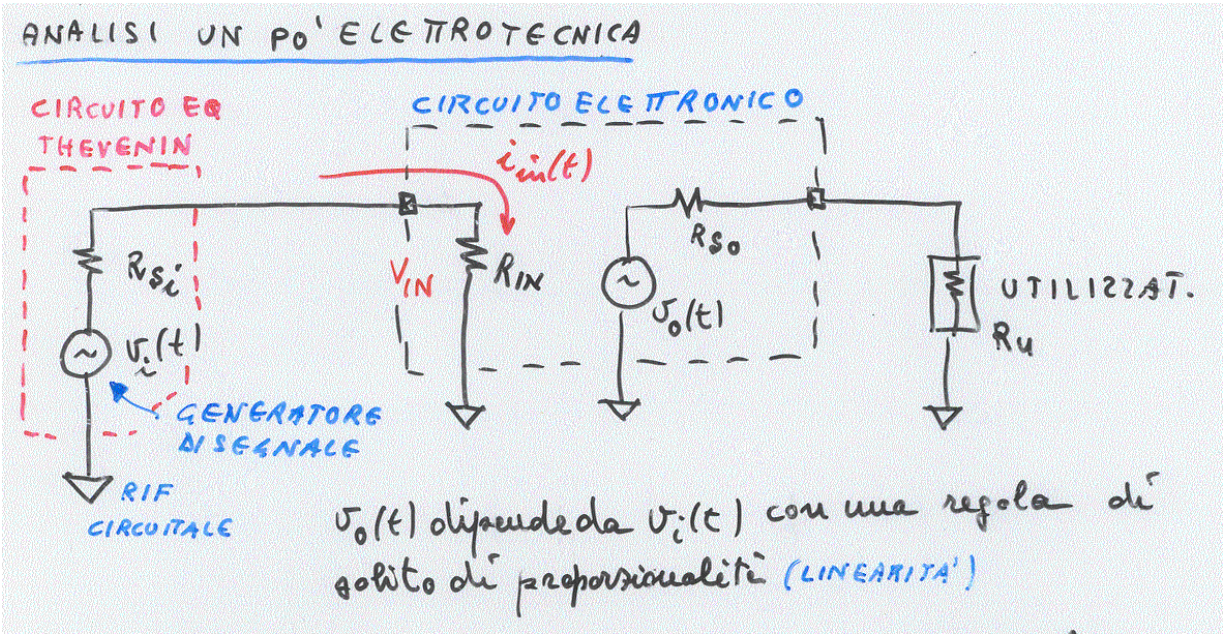


Figure 21. Thevenin source and receiver input represented as one electrical interconnection.

The current and the voltage actually presented to the electronics are therefore

$$i_{IN}(t) = \frac{v_i(t)}{R_{si} + R_{IN}}, \tag{87}$$

$$V_{IN}(t) = v_i(t)\frac{R_{IN}}{R_{si} + R_{IN}}. \tag{88}$$

The intended condition $V_{IN} = v_i$ is reached exactly only in either of two ideal limits: $R_{si} = 0$, meaning an ideal voltage source, or $R_{IN} \to \infty$, meaning a receiver that draws no current. A real sensor has a non-zero output resistance that cannot simply be removed. Consequently, voltage-mode measurement electronics is normally designed so that

$$R_{IN} \gg R_{si}. \tag{89}$$

This makes loading error small. If an admissible fractional attenuation is ε, then

$$\frac{V_{IN}}{v_i} = \frac{1}{1 + R_{si}/R_{IN}} \geq 1 - \varepsilon, \tag{90}$$

which, for small ε, requires approximately $R_{IN} \geq R_{si}/\varepsilon$. A 1% loading target therefore calls for an input resistance of roughly one hundred times the source resistance.

The same system-level model applies at the output of a conditioning stage. A real output stage has an output resistance and drives a finite load. Good measurement-interface design therefore aims for a high input resistance to avoid disturbing the sensor and a low output resistance to make the conditioned voltage insensitive to the next stage.

The high input resistance that solves the loading problem creates another difficulty: the input becomes sensitive to small currents coupled from the environment. High R_{IN} protects the wanted source voltage, but it also allows an unwanted source to develop a substantial voltage at the input.

5.2.A general model of coupled electrical interference

An unwanted disturbance can also be represented by a Thevenin source $e(t)$ and a source or coupling resistance R_d. If it is connected to the receiver input, the coupled voltage is

$$v_x(t) = e(t)\frac{R_{IN}}{R_d + R_{IN}}. \tag{91}$$

If $R_{IN} \gg R_d$, then $v_x \simeq e$: precisely the high impedance selected to minimize sensor loading may allow most of the disturbance voltage to appear at the receiver. This is not an argument for arbitrarily lowering R_{IN}. It is the motivation for controlling the coupling path, using balanced/differential transmission, and arranging shielding and grounding correctly.

Two physical coupling mechanisms must be separated:

1. electric-field coupling, represented by parasitic capacitances;
2. magnetic-field coupling, represented by induced electromotive force in a loop.

They require different countermeasures. A conductive electrostatic shield is highly effective against capacitive coupling but, particularly at power-line frequencies, ordinary copper shielding does not by itself eliminate magnetic induction.

5.3.Capacitive coupling from an external voltage

Two conductors separated by an insulator form a capacitor. The parallel-plate expression

$$C = \varepsilon \frac{S}{d} \tag{92}$$

is introduced as the simplest geometric model: capacitance increases with facing area S and permittivity ε, and decreases with separation d. Cable geometry is not a parallel-plate geometry, but the same dependence remains useful qualitatively.

The area, separation and permittivity dependence is shown in Figure 22.

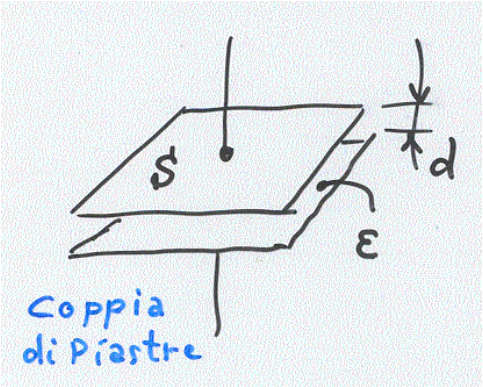


Figure 22. Geometrical origin of parasitic capacitive coupling between two conductors.

A power conductor and a signal conductor, or two adjacent cables, possess a distributed mutual capacitance.

At angular frequency ω, the capacitive impedance is

$$Z_C = \frac{1}{j\omega C} = \frac{1}{j2\pi f C}, \quad |Z_C| = \frac{1}{2\pi f C}. \tag{93}$$

For a disturbance source e coupled through C into an input resistance R_{IN}, the complete complex divider is

$$V_x = E\frac{R_{IN}}{R_d + Z_C + R_{IN}}, \tag{94}$$

where R_d represents any additional source-path resistance. Neglecting R_d, a larger R_{IN} moves V_x closer to the interference voltage. A lower frequency or smaller capacitance raises $|Z_C|$ and reduces coupling.

A representative scale calculation considers two conductors running for several tens of metres at centimetre-scale separation, with a total parasitic capacitance of approximately 300-400 pF. For $C = 300\ \text{pF}$ at $f = 50\ \text{Hz}$,

$$|Z_C| = \frac{1}{2\pi(50)(300\times10^{-12})} \simeq 10.6\ \text{M}\Omega. \tag{95}$$

If a 220 V mains conductor couples through that capacitance into a $100\ \text{k}\Omega$ input, the approximate interference voltage is

$$V_x \simeq 220\frac{100\ \text{k}\Omega}{10.6\ \text{M}\Omega + 100\ \text{k}\Omega} \simeq 2.1\ \text{V}. \tag{96}$$

The result is only about one hundredth of the mains voltage, but it is very large compared with a typical low-level analogue signal.

The corresponding 50 Hz coupling equivalent is shown in Figure 23.

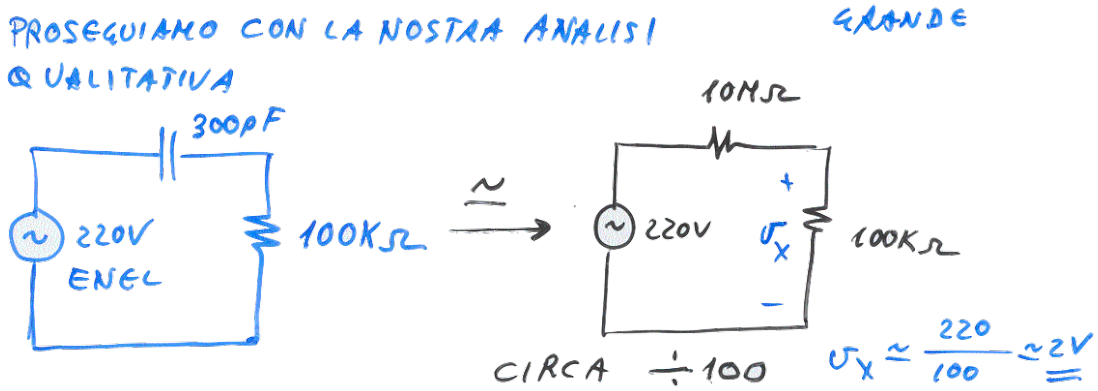


Figure 23. Compact mains-frequency capacitive-coupling equivalent applied to a high-impedance sensor input.

In the second numerical comparison, a $350\ \Omega$ load-cell source subjected to an equivalent $10\ \text{M}\Omega$ interference path develops approximately

$$220\frac{350}{10^7 + 350} \simeq 7.7\ \text{mV}, \tag{97}$$

which is already a substantial fraction of a 20 mV full-scale sensor output. The lesson is relative rather than absolute: a coupled voltage that appears negligible relative to the external power system can dominate the measurement.

5.4.Differential signals and common-mode interference

Consider two signal conductors routed close together and exposed to the same external electric field. If their geometry relative to the disturbing conductor is nearly equal, their coupling capacitances are approximately equal. The resulting disturbance voltages are then nearly the same on both signal conductors.

The close-pair geometry is shown in Figure 24.

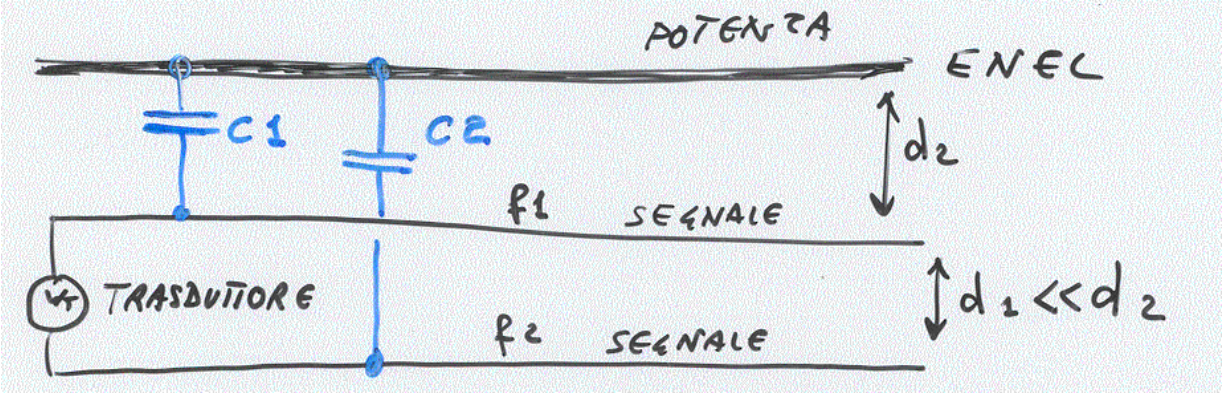


Figure 24. Closely spaced signal conductors exposed to approximately the same external electric field.

Any pair of input voltages can be written as

$$V_A = v_{CM} + \frac{v_d}{2}, \quad V_B = v_{CM} - \frac{v_d}{2}, \tag{98}$$

with

$$v_d = V_A - V_B, \quad v_{CM} = \frac{V_A + V_B}{2}. \tag{99}$$

An ideal differential receiver produces

$$V_{out} = K(V_A - V_B) = K v_d . \tag{100}$$

If the same disturbance $e(t)$ appears at both inputs, then it cancels algebraically:

Equal coupled voltages at the two inputs are shown in Figure 25.

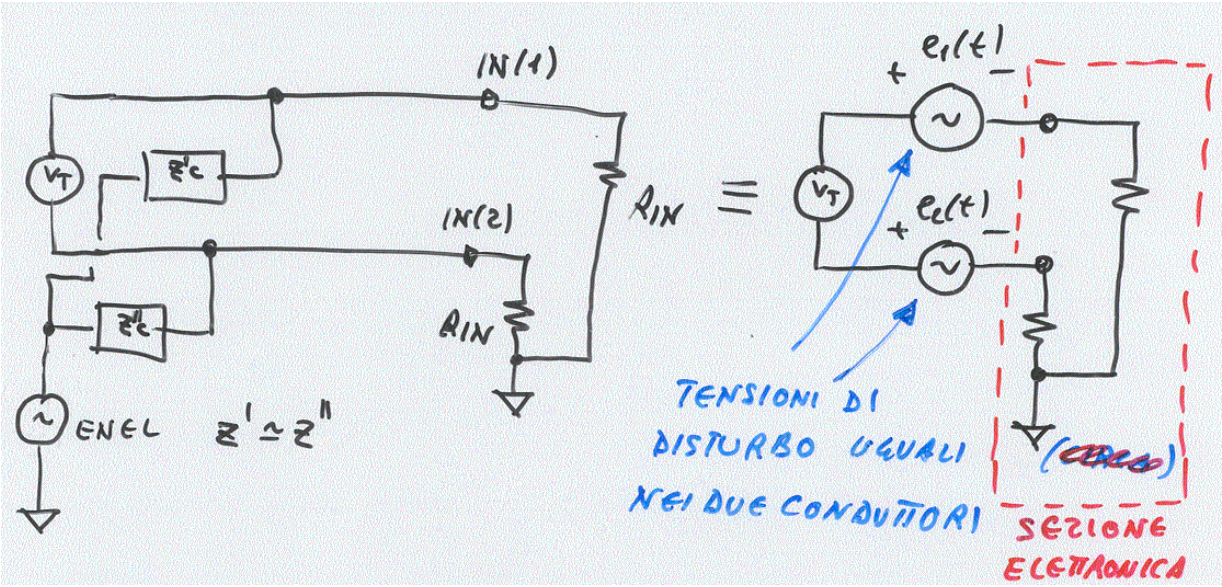


Figure 25. Equal interference voltages applied to both inputs of a differential receiver.

$$V_{\text{out}} = K[(V_A + e) - (V_B + e)] = K(V_A - V_B). \tag{101}$$

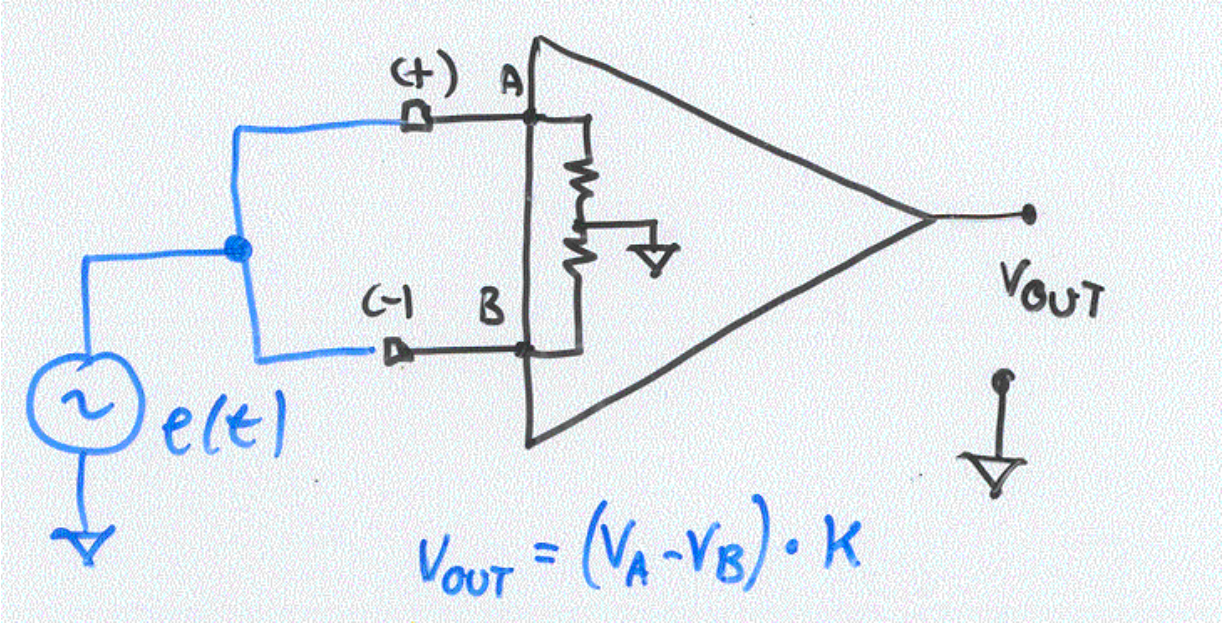
Figure 26 separates the two cases. In panel (a), the same disturbance drives both inputs and the differential voltage is zero. Panel (b) adds the wanted transducer voltage V_T to the connection. With the source polarities indicated in the drawing, the received voltage is

$$V_{AB} = e' + V_T - e'' = V_T + (e' - e'')\,. \tag{102}$$

If the two coupled disturbances are equal, their difference vanishes and the wanted sensor voltage remains:

$$e' \simeq e'' \;\Rightarrow\; V_{AB} \simeq V_T, \quad V_{\text{out}} \simeq K\,V_T\,. \tag{103}$$

(a) Common-mode voltage alone



(b) Sensor voltage with coupled interference

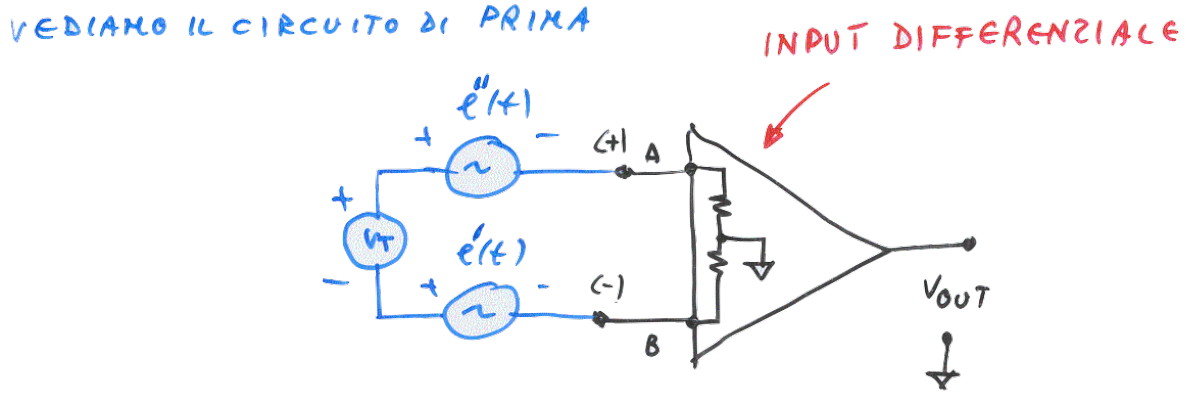


Figure 26. Common-mode rejection: (a) equal input voltages without a sensor signal; (b) a sensor voltage with disturbances on both conductors.

Any mismatch in cable capacitance, conductor resistance, source impedance, or receiver input impedance converts a portion of common-mode interference into differential error. Moreover, common-mode cancellation does not mean that the voltage has disappeared from the input terminals. Both terminals can still be at a large voltage relative to the receiver ground. A practical amplifier must keep this voltage inside its permitted common-mode input range and must have enough common-mode rejection ratio at the interference frequency.

For a real differential amplifier,

$$V_{out} = A_d v_d + A_{CM} v_{CM}, \tag{104}$$

and

$$\mathrm{CMRR} = \left| \frac{A_d}{A_{CM}} \right|, \quad \mathrm{CMRR}_{dB} = 20\log_{10} \left| \frac{A_d}{A_{CM}} \right|. \tag{105}$$

The residual output due to common mode is $A_{CM} v_{CM} = A_d v_{CM} / \mathrm{CMRR}$. High CMRR is therefore essential, but it cannot repair a common-mode input voltage that exceeds the amplifier's allowed range.

5.5.Electrostatic shielding, return-current control, and grounding

A conductive shield intercepts electric-field coupling and needs a defined return for the resulting displacement current. The return must be chosen together with the signal reference. Figure 27 exposes the potential ground loop: a voltage between the remote and local ground points can drive current through their connecting shield or return.

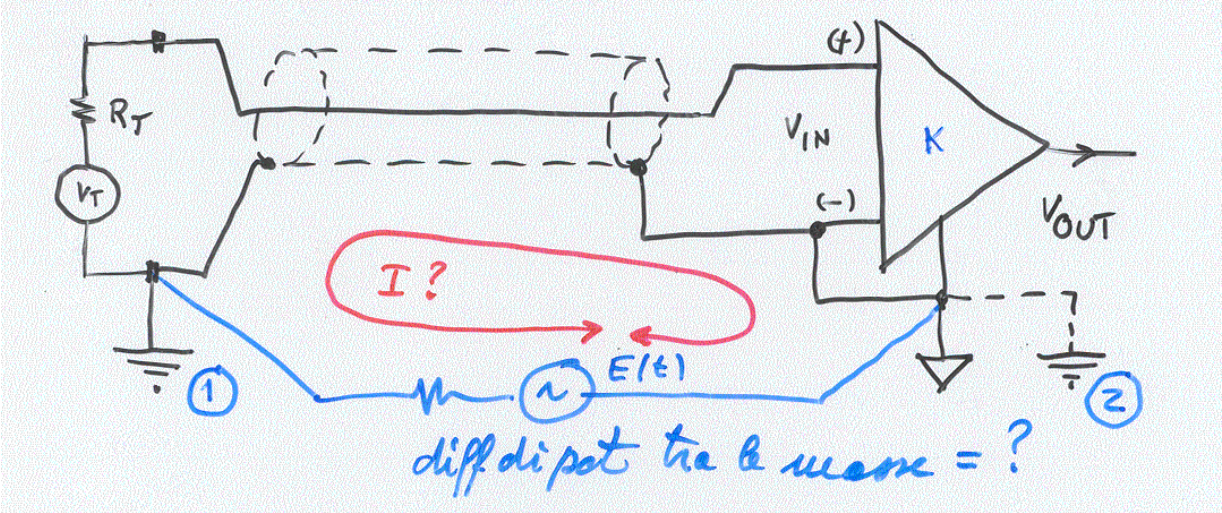


Figure 27. Shield-current return path and its relation to the signal reference.

The relevant parasitic elements in the equivalent circuit are the capacitance C_{ES} between the external source and shield, the shield-to-conductor capacitances C_{S1} and C_{S2}, and the inter-conductor capacitance C_{12}. The shield works electrically because it controls the field and supplies a low-impedance return for coupled current; a metal enclosure alone is not sufficient if it is left floating.

The relevant parasitic coupling paths are identified in Figure 28.

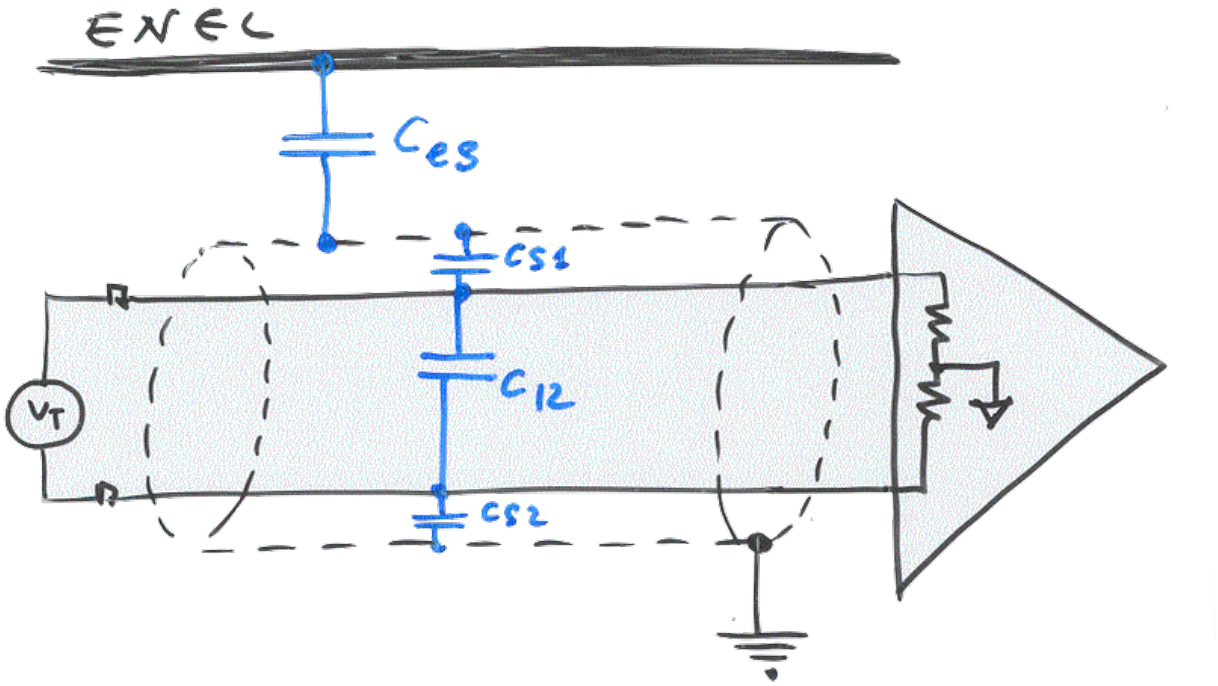


Figure 28. Capacitive coupling paths between an enclosure, shielded conductors and a differential receiver.

With an ungrounded or poorly referenced shield, the external source can drive the shield through C_{ES}. The floating physical arrangement is shown in Figure 29.

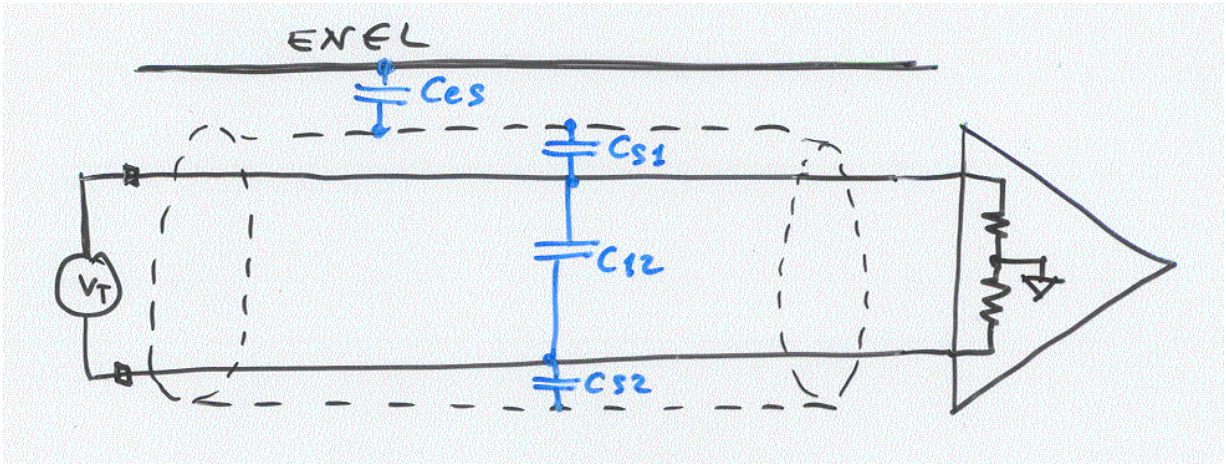


Figure 29. Floating shield inserted between an external electric field and a differential signal pair.

Its equivalent capacitive network is shown in Figure 30.

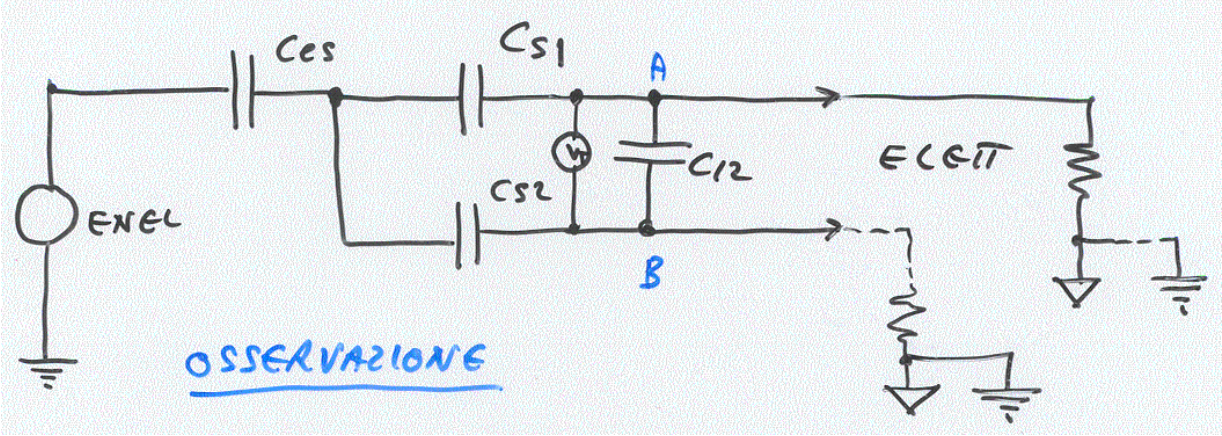


Figure 30. Equivalent capacitive network of a floating shield and two signal conductors.

The shield voltage then couples through C_{S1} and C_{S2} to both internal conductors. If the geometry is perfectly balanced this voltage is principally common mode and the differential receiver may reject it, but it still consumes common-mode range and any imbalance produces a differential residue. An interference generator should not be modelled as an ideal zero-impedance voltage source: a series coupling impedance R_d, or the actual capacitive impedance, is essential to determine how grounding attenuates it.

The ground arrangement determines where interference current flows. In a single-ended circuit with a shared signal return, the received voltage may be written schematically as

$$V_{in} = V_T + e'' - e' - I_{in} \sum R_i \,. \tag{106}$$

If $e' \simeq e''$ and $I_{\text{in}} \simeq 0$, cancellation is possible. It is fragile, however, because it depends on equal coupling and negligible receiver current.

Figure 31 shows the two disturbance paths before bonding. A low-resistance bond between the reference points, as in Figure 32, attenuates the return-conductor disturbance:

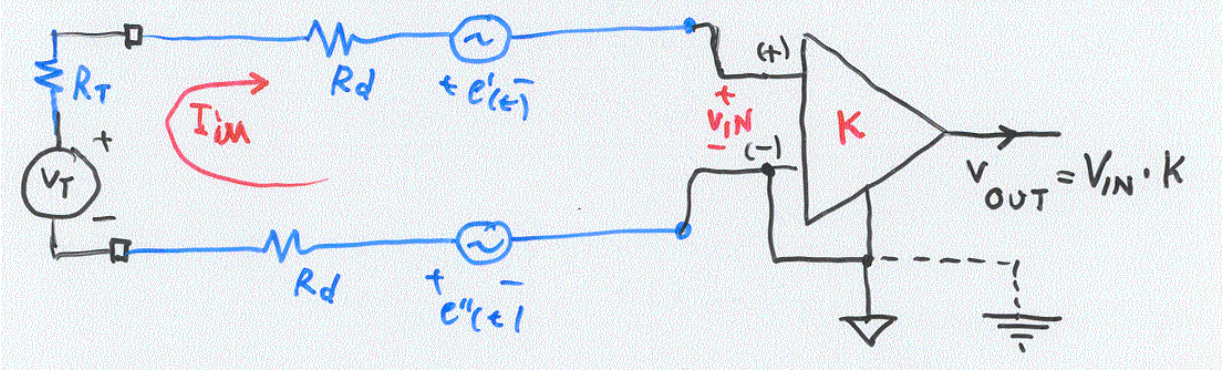


Figure 31. Single-ended receiver with coupled disturbance sources and resistances in both conductors.

$$V_{xy} \simeq e'' \frac{R_{MM}}{R_d + R_{MM}} \ll e'' \text{ when } R_{MM} \ll R_d \,. \tag{107}$$

That bond does not automatically eliminate every other coupled source.

The attenuation produced by the shield bond is shown in Figure 32.

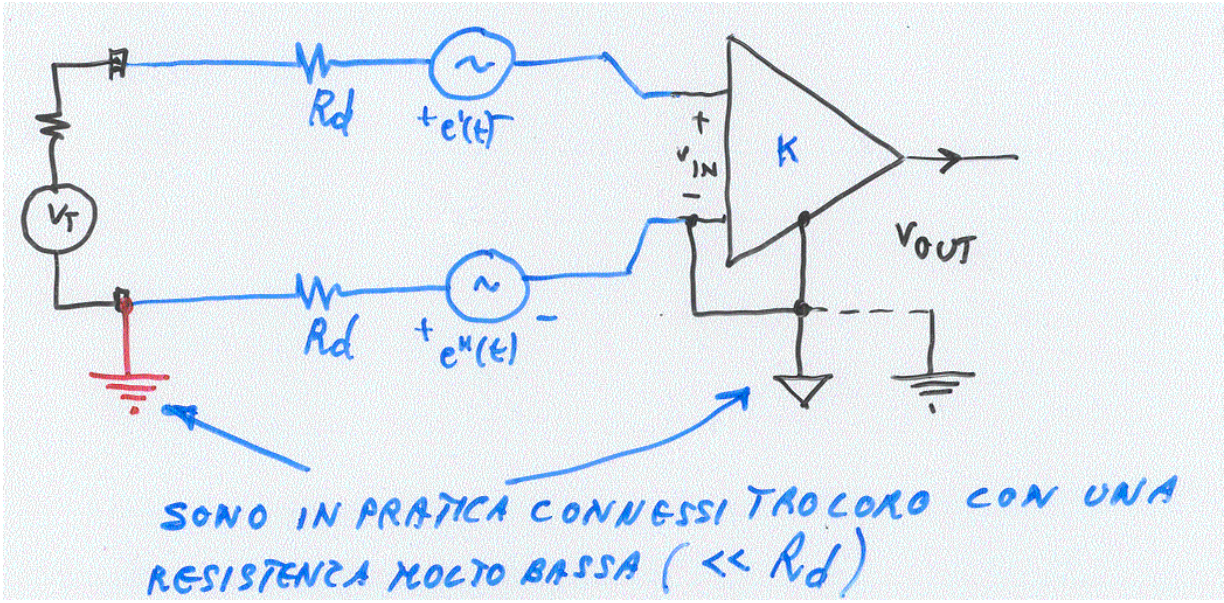


Figure 32. Low-resistance bond between the source and receiver reference points.

Figure 33 shows the low-resistance bond attenuating the disturbance on the reference conductor. The residual equivalent source on that conductor approaches zero when the bond resistance is small compared with the coupling resistance.

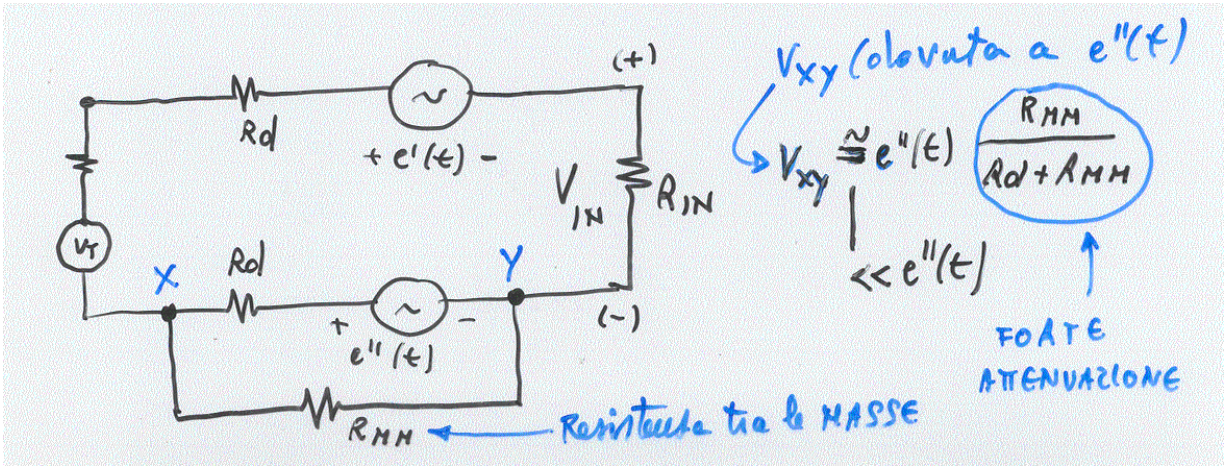


Figure 33. Attenuation of the reference-conductor disturbance by a low-resistance bond.

The other coupled source remains in the signal conductor. Figure 34 therefore gives $V_{\mathrm{in}} \simeq V_T - e'(t)$ when the receiver current and the reference-conductor residue are negligible. Grounding one path has not restored equal disturbance voltages at the two input terminals.

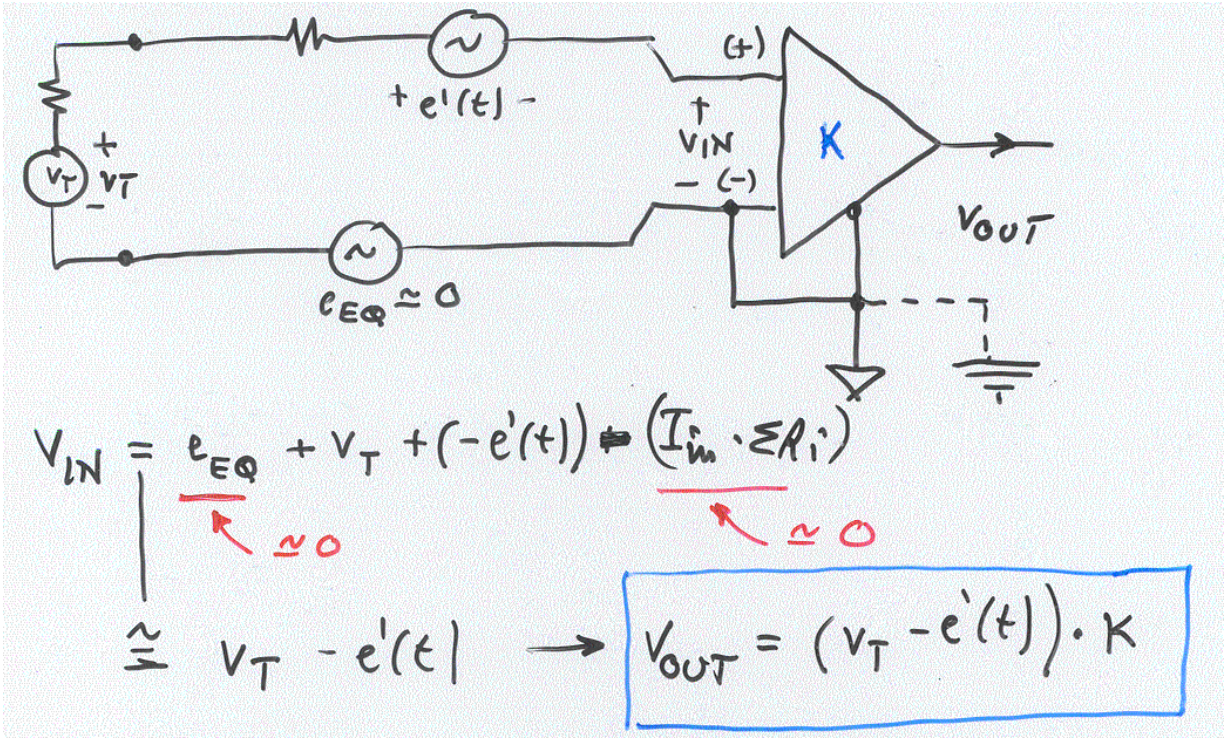


Figure 34. Residual differential interference after the reference-conductor disturbance has been attenuated.

The cable arrangement in Figure 35 uses the coaxial shield as the signal-return conductor. The shield surrounds and electrostatically protects the centre conductor, as stated by the blue note, but it also belongs to the measurement circuit. Any shield voltage drop is consequently part of the voltage delivered to the receiver.

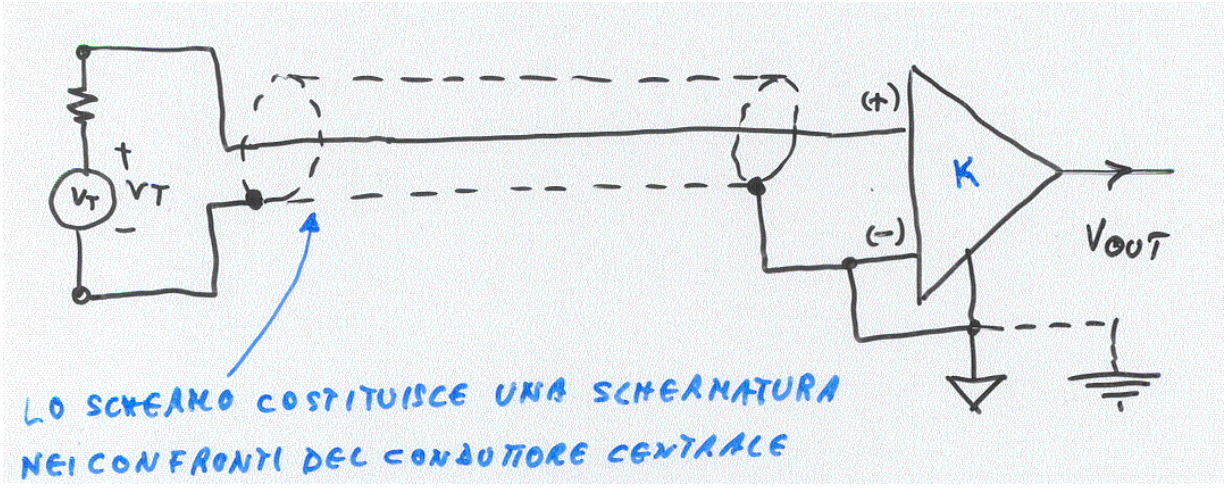


Figure 35. Coaxial connection with the shield serving as the signal-return conductor.

A shielded two-conductor cable separates these roles: the inner pair carries the signal and its return, while the shield has a separate protective-current path. Figure 36 compares the favourable case, where shield current is nearly zero, with a shared return that admits disturbance current. The improvement comes from separating the paths rather than merely adding metal around the cable.

The favourable and unfavourable current routes are compared in Figure 36.

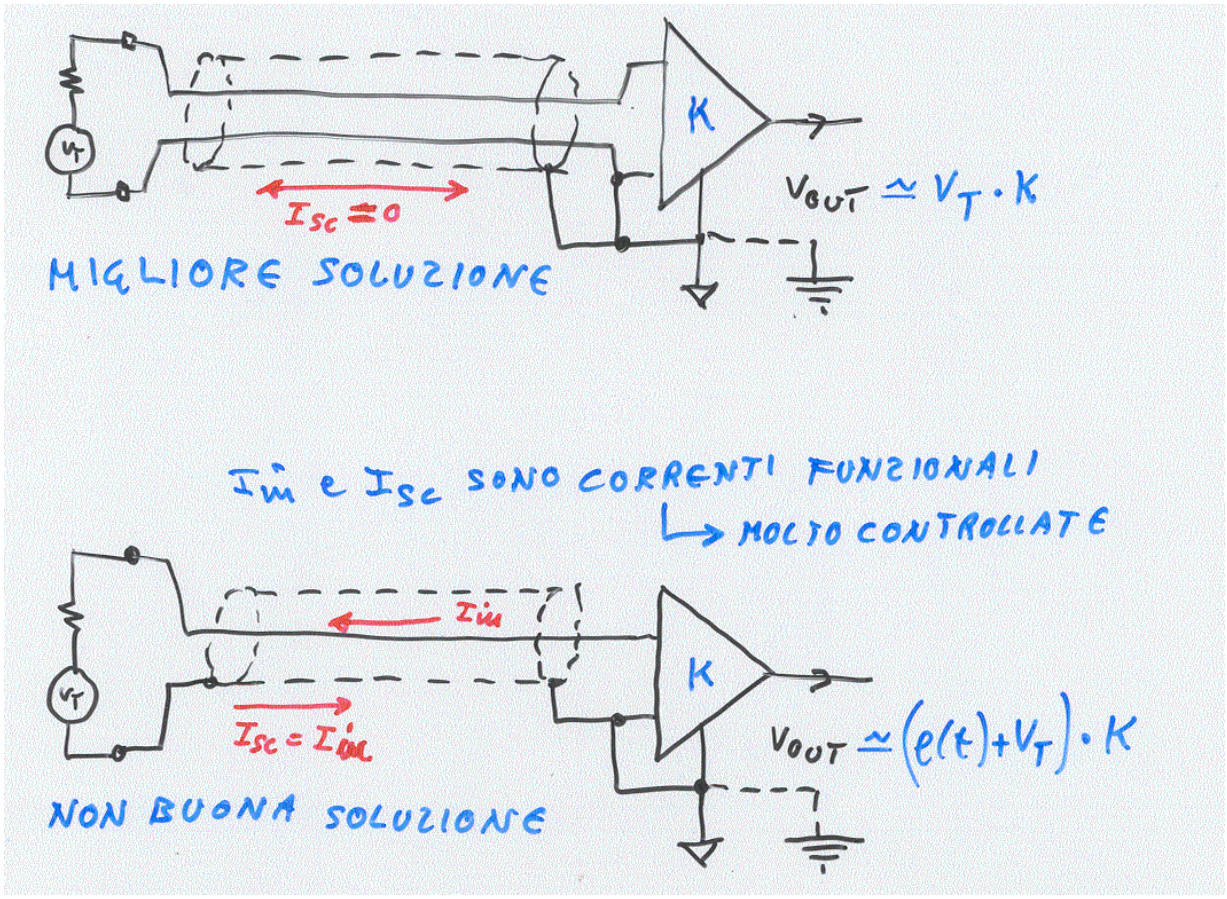


Figure 36. Comparison of shield-current routes with favourable and unfavourable signal-reference coupling.

Connecting a shield to ground at both ends can produce a loop if the two ground points are at different potentials. A voltage $E(t)$ between the ground points then drives shield current.

The conductive loop created by two-end grounding is shown in Figure 37.

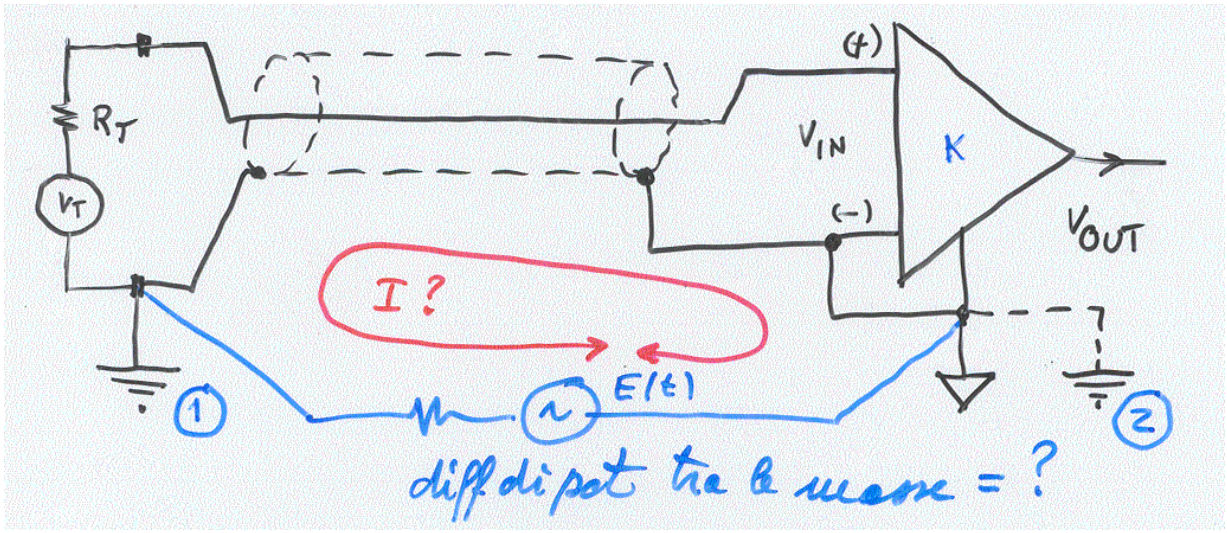


Figure 37. Shield bonded at both ends between separated reference potentials.

Keeping that current separate from the two signal conductors prevents it from becoming part of the wanted differential signal.

The separated shield- and signal-current paths are shown in Figure 38.

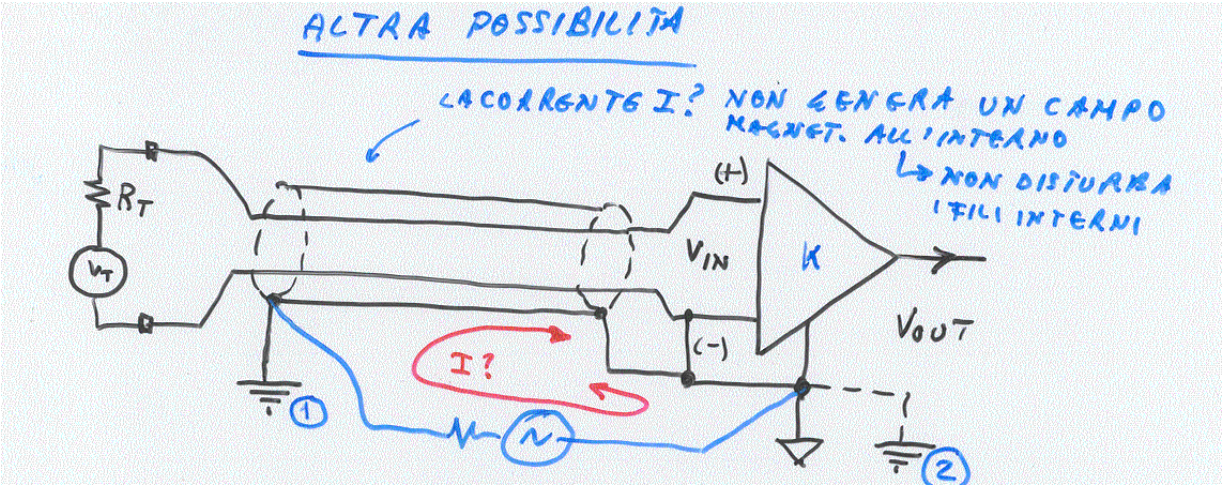


Figure 38. Separate shield-current route preventing shield current from sharing the signal return.

5.6.Magnetic coupling and loop-area reduction

A time-varying current creates a time-varying magnetic field.

The field linked by a nearby conductor loop is shown in Figure 39.

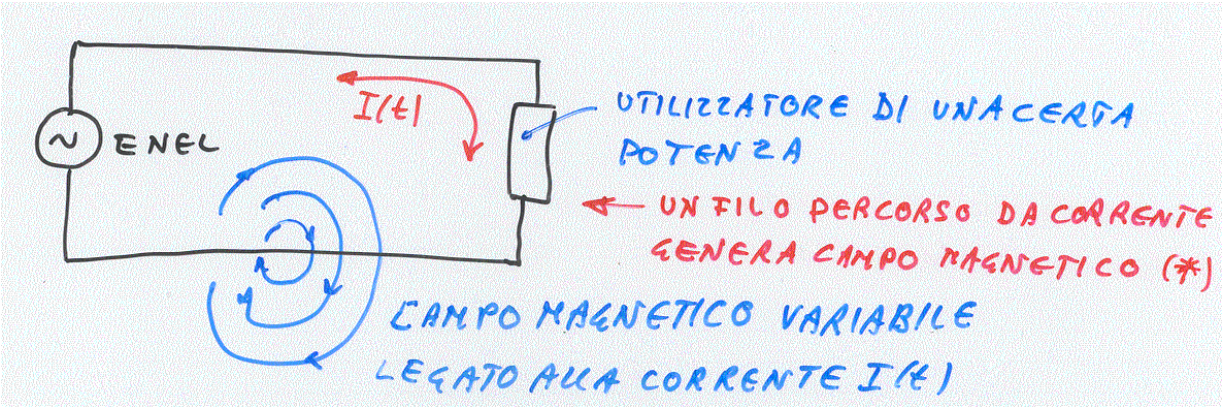


Figure 39. Magnetic field produced by a current loop and linked to nearby wiring.

If magnetic flux crosses the loop formed by the outgoing and return signal conductors, Faraday's law gives the induced electromotive force

$$e_{ind}(t) = -\frac{d\Phi(t)}{dt}, \quad \Phi(t) = \int_S \boldsymbol{B}(t) \cdot d\boldsymbol{S}\,. \tag{108}$$

For an approximately uniform field normal to a loop of area A,

$$e_{ind}(t) \simeq -A\frac{dB(t)}{dt}\,. \tag{109}$$

The induced voltage therefore increases with loop area, field magnitude, field-change rate, and the component of the field normal to the loop. Unlike a capacitively coupled disturbance that appears equally on both conductors, a magnetically induced loop voltage is a genuine differential voltage. In the simplified measurement chain,

$$V_{in} \simeq V_T + e_{ind}, \quad V_{out} \simeq K(V_T + e_{ind})\,. \tag{110}$$

An ideal differential amplifier cannot reject it because the error is already part of v_d.

The induced differential series voltage is shown in Figure 40.

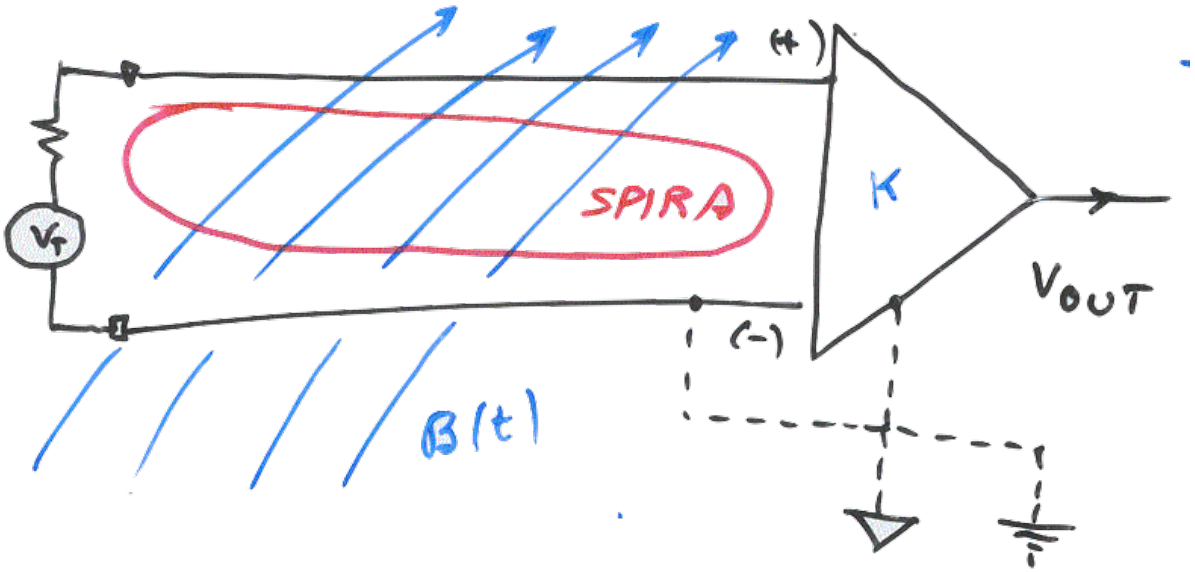


Figure 40. Magnetically induced series voltage applied to a differential receiver.

Increasing separation from the disturbing current reduces magnetic coupling. Keeping the outgoing and return conductors close together also reduces the enclosed loop area and promotes cancellation of their external fields.

The field cancellation of a close opposing-current pair is shown in Figure 41.

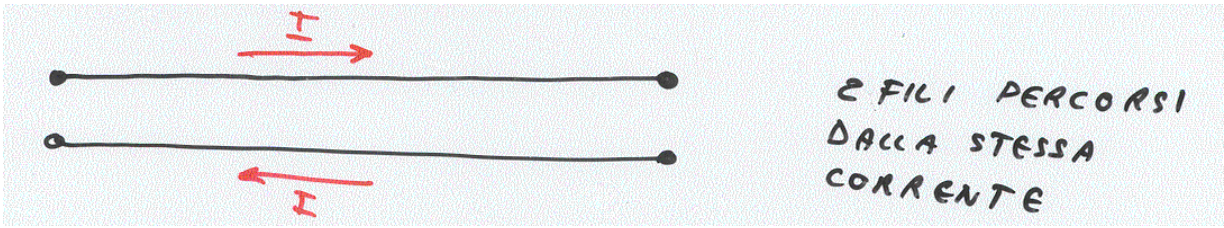


Figure 41. Adjacent conductors carrying equal and opposite currents.

An ordinary electrostatic shield does not by itself eliminate an externally applied magnetic field; the illustrated magnetic shield instead guides flux around the protected conductors.

Magnetic-flux diversion around the protected cable is shown in Figure 42.



Figure 42. Magnetic-field diversion around a cable by a high-permeability cylindrical shield.

Twisting repeatedly exchanges the physical positions of the two conductors. The signal path and its return then enclose a sequence of small loops whose oriented areas alternate in sign, as shown in Figure 43. Keeping the wires close also reduces the magnitude of each loop area.

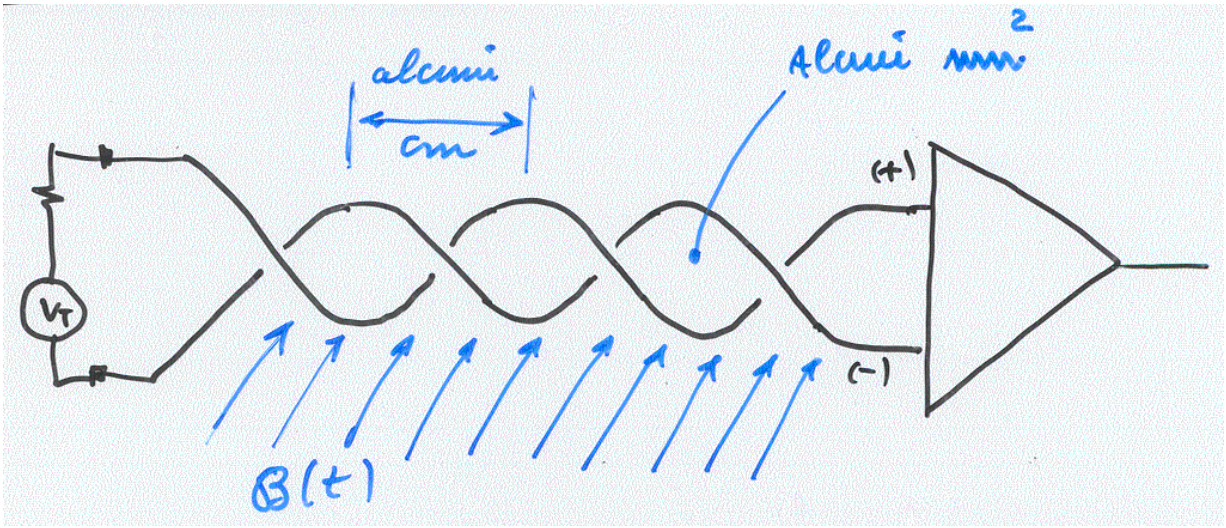


Figure 43. Twisted-pair geometry reducing net magnetic pickup at a differential receiver.

Use the same terminal polarity, from A to B, when comparing adjacent loops. If they have equal area and the magnetic field is effectively uniform over their separation, they link equal flux magnitudes with opposite orientations. Figure 44 illustrates the corresponding equal-and-opposite induced voltages:

$$v'_{AB}(t) = -\,v''_{AB}(t), \quad v_{AB,\mathrm{pair}}(t) = v'_{AB}(t) + v''_{AB}(t) = 0\,. \tag{111}$$

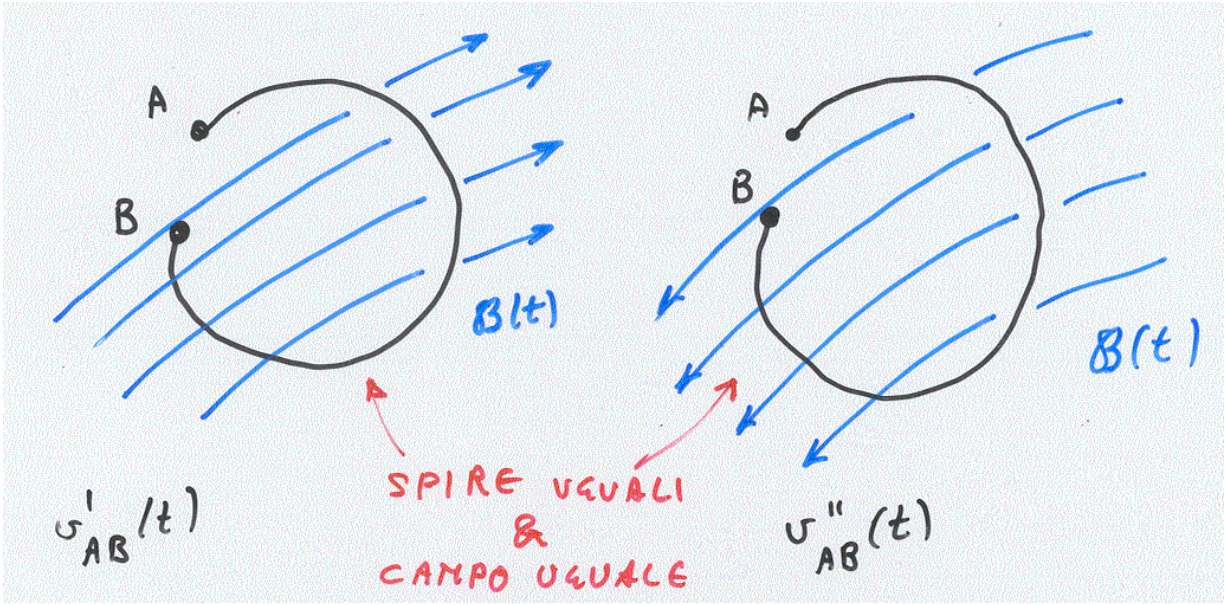


Figure 44. Opposed conductor loops exposed to the same time-varying magnetic field.

The equality is exact for the ideal matched-loop construction. In a real twisted pair, cancellation is approximate because the field and the loop geometry are not perfectly uniform. A shorter twist pitch makes adjacent loops sample more nearly the same field and limits the uncancelled area at the ends. Field gradients, irregular spacing and untwisted connector leads leave a residual. Differential reception cannot remove that residual magnetic voltage once it is part of the signal difference; it rejects the common-mode voltage coupled similarly onto both wires.

The combined electric- and magnetic-field countermeasures are shown in Figure 45.

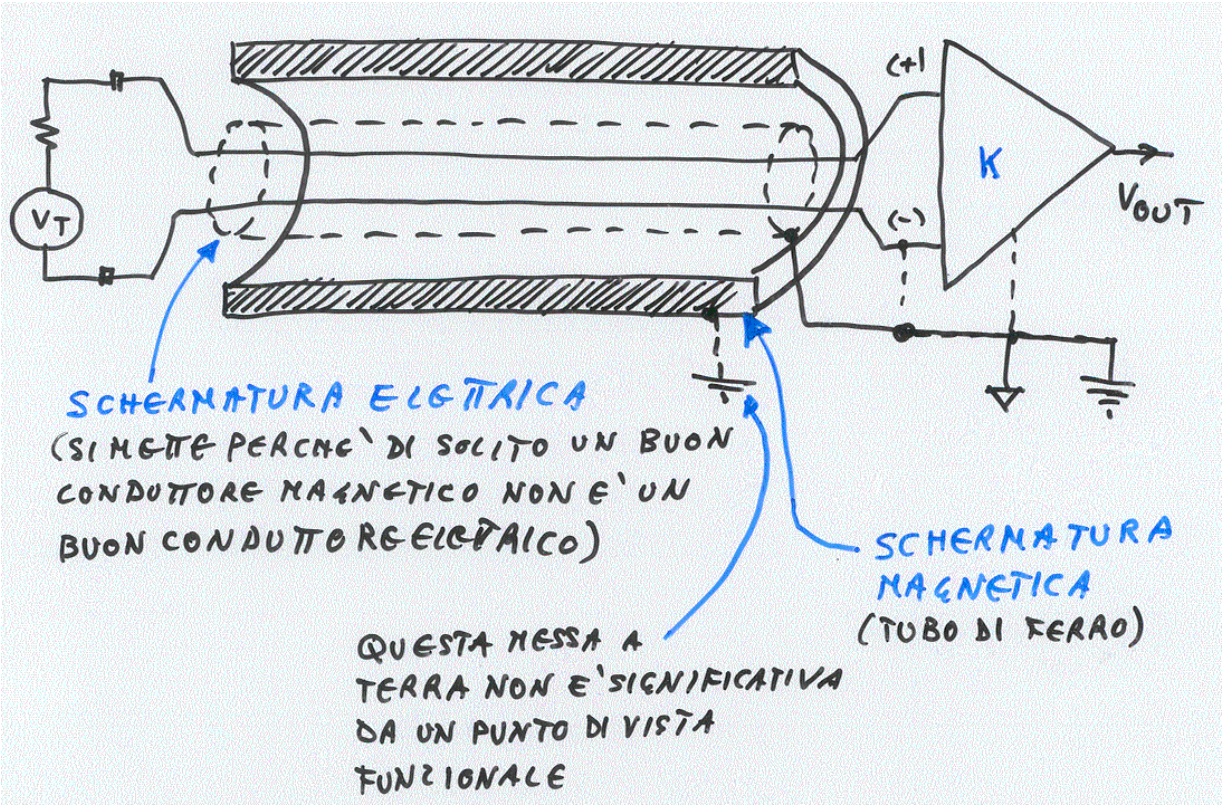


Figure 45. Combined electric and magnetic shielding around a remote differential connection.

5.7.Remote sensing and industrial current transmission

The same principles apply directly to remote transducers.

5.7.1.Four-wire voltage sensing

A powered transducer can use two conductors for excitation or power and a separate twisted pair for sensing. Conductors F_1 and F_2 carry the supply current I_{ALIM}, while F_3 and F_4 connect the transducer output directly to a differential amplifier. Because the amplifier input currents are approximately zero, there is almost no voltage drop in the sense conductors. The receiver measures the voltage at the transducer terminals rather than a voltage shifted by the drop in a power-return conductor.

The separate force and sense paths are shown in Figure 46.

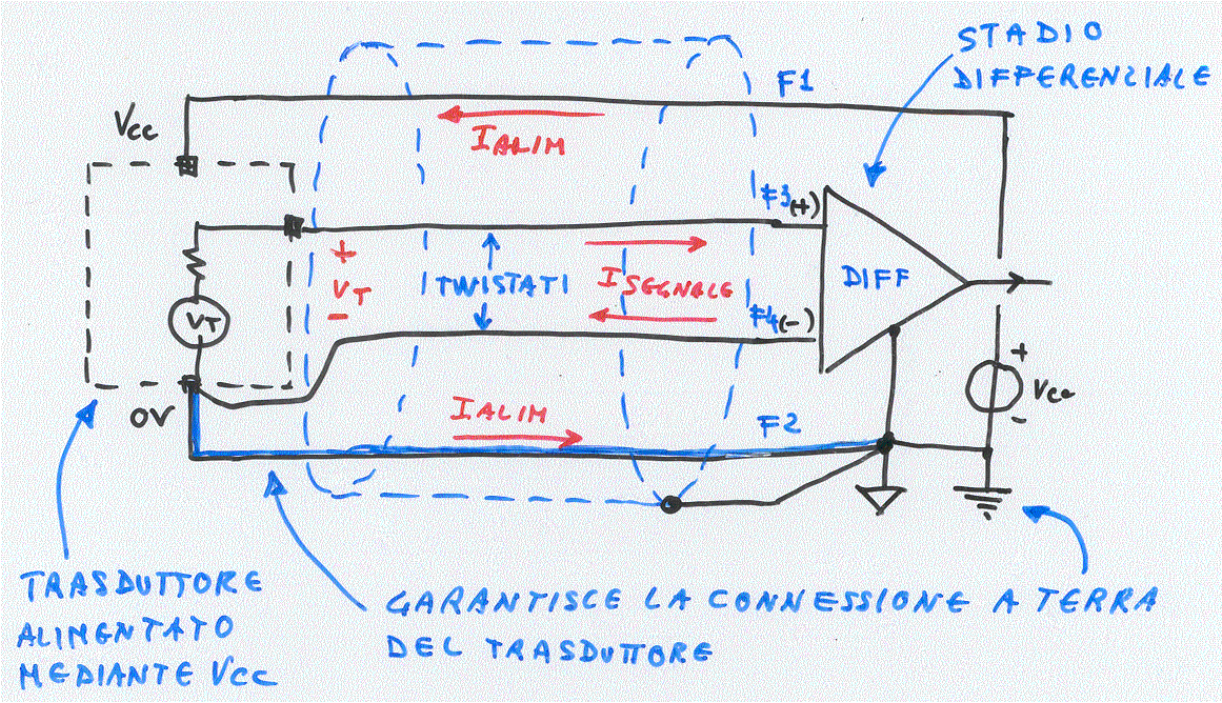


Figure 46. Remote powered sensor with separate supply, signal and reference-current paths.

If one sense lead is omitted and the receiver instead references the signal to its local ground, the measured value can become

$$V_{meas} = V_T + I_{ALIM} R_{F2}, \tag{112}$$

with sign depending on the adopted polarity. The supply-wire voltage drop has then entered the measurement. The separate sense pair is the voltage-measurement analogue of a Kelvin connection: conductors that carry appreciable current are not reused as precision voltage references.

5.7.2.Two-wire 4-20 mA transmission

A loop-powered transmitter provides an alternative. The total loop current is decomposed conceptually as

$$I = J_1 + J_2, \tag{113}$$

where $J_2 \simeq 4\ \mathrm{mA}$ powers the transmitter electronics and J_1 varies from approximately 0 to 16 mA with the measurand.

The live-zero and variable-current contributions are shown in Figure 47.

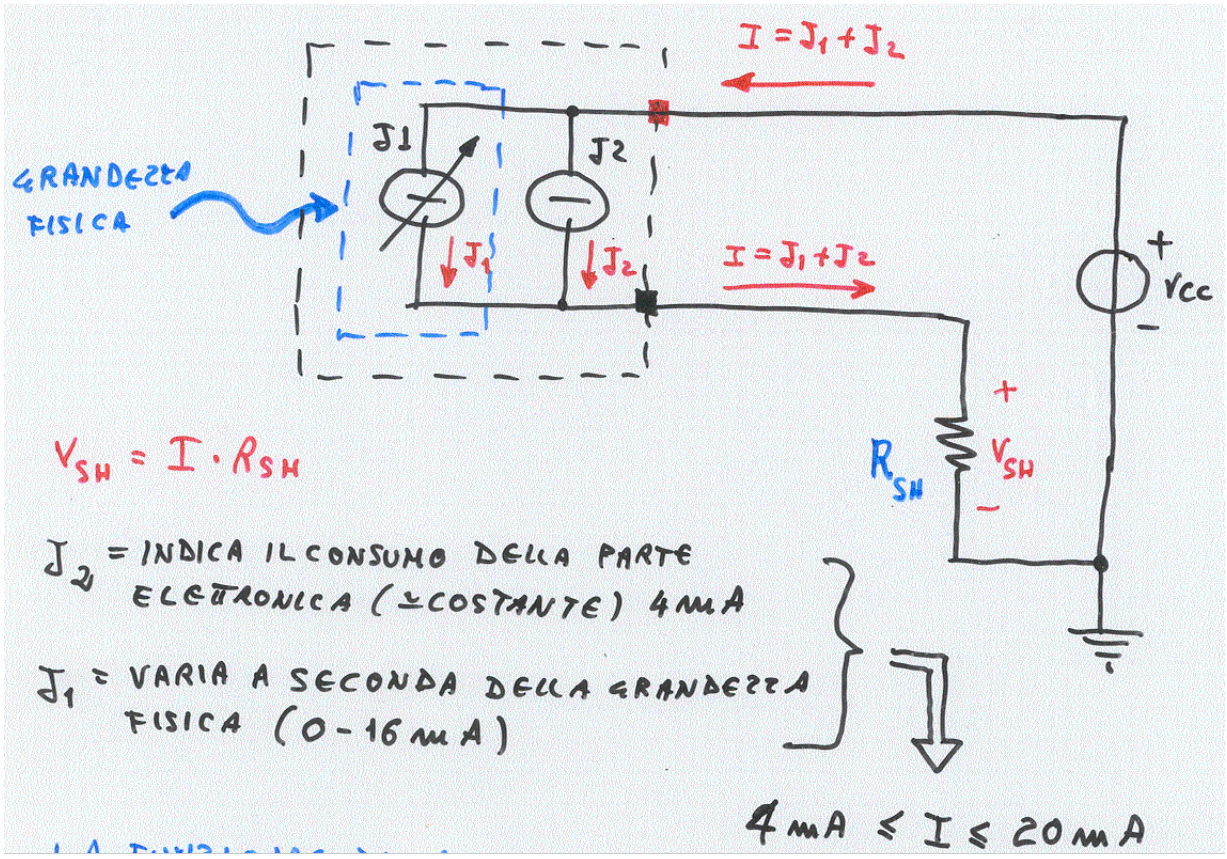


Figure 47. Powered 4-20 mA transducer represented as variable signal current plus constant electronic current.

Thus

$$4\ \text{mA} \le I \le 20\ \text{mA}\,. \tag{114}$$

A receiver converts the current into a voltage with a shunt resistor R_{SH}:

$$V_{SH} = IR_{SH}\,. \tag{115}$$

If a subsequent stage has gain K',

$$V_{out} = IR_{SH}K'\,. \tag{116}$$

The non-zero 4 mA lower endpoint provides a live zero: it can power the remote electronics and allows a zero-current open circuit to be distinguished from a valid minimum measurement. Current transmission is comparatively insensitive to series wire resistance as long as the source retains enough compliance voltage to force the commanded current through the complete loop.

5.8.Input RF suppression, overload prevention, and symmetrical protection

Unwanted input content falls into two classes:

- relatively small out-of-band components, which can be attenuated by a linear filter; and
- potentially large transient or radio-frequency components, which can drive an unprotected amplifier out of its linear region.

This distinction is fundamental. It is incorrect to place a low-pass filter after a real amplifier and assume that all high-frequency interference has been removed. The amplifier first receives the sum of the wanted and unwanted components. If an out-of-band component causes clipping, slew-rate limiting, input-stage rectification, or intermodulation, the resulting low-frequency products lie inside the useful band and cannot be removed afterward. The input must therefore contain both a linear filtering function and a nonlinear limiting or protection function.

5.8.1.Symmetric passive RC input filter

A basic symmetric input filter places an equal series resistor and equal shunt capacitor in each lead. The matched two-path input cell is shown in Figure 48.

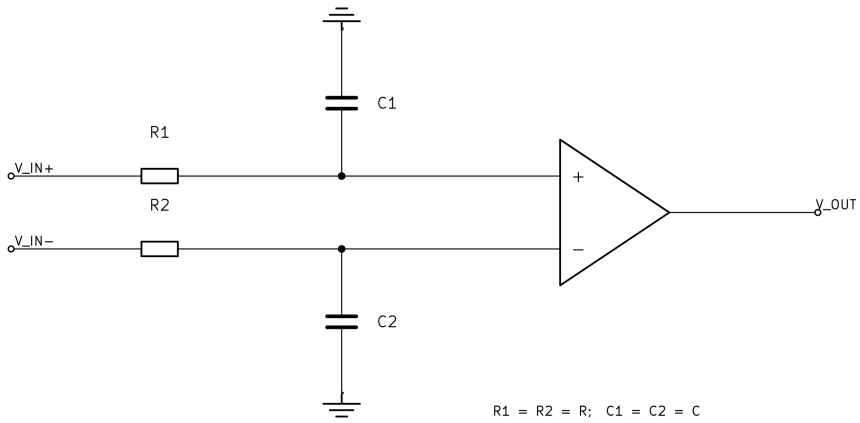


Figure 48. Matched differential-input RC filter preserving symmetry between the two conductors.

For a high-impedance amplifier and low-impedance source, each path has

$$H(s) = \frac{1}{1 + sRC}, \quad f_c = \frac{1}{2\pi RC}. \tag{117}$$

The network must satisfy four conditions:

- negligible alteration of the wanted differential signal;
- negligible change to the source loading within the wanted band;
- strong attenuation of unwanted higher-frequency components before they reach a nonlinear device;
- close equality between the two paths so that common-mode interference remains common mode.

If the two paths have transfer functions $H_+(s)$ and $H_-(s)$, a common input v_{cm} produces a differential error

$$v_{d,err}(s) = [H_+(s) - H_-(s)]v_{cm}(s). \tag{118}$$

The equality of time constants is therefore a CMRR requirement, not merely a cutoff-frequency requirement. Matched components and symmetrical layout matter most near the RC corner, where small differences in R or C cause the largest phase and magnitude mismatch.

The two paths must use equal time constants so that a common disturbance remains common mode at the amplifier inputs. In the illustrated example, $R = 10\,\mathrm{k\Omega}$ and $C = 1\,\mathrm{nF}$ give $f_c \simeq 15.9\,\mathrm{kHz}$ and an input-impedance magnitude of approximately $160\,\mathrm{k\Omega}$ at $1\,\mathrm{kHz}$. This passive cell precedes the active input; accurate measurement-band filtering is applied after buffering.

5.8.2.Input limiting and protection

A single diode referenced to a fixed positive voltage acts as a one-sided limiter. Below approximately $V_{MAX} + V_F$ it is off and the circuit is transparent; above that threshold it conducts and clamps the node. A complete differential input requires protection against both polarities and essentially identical networks in the two leads.

The symmetrical bipolar limiter is shown in Figure 49.

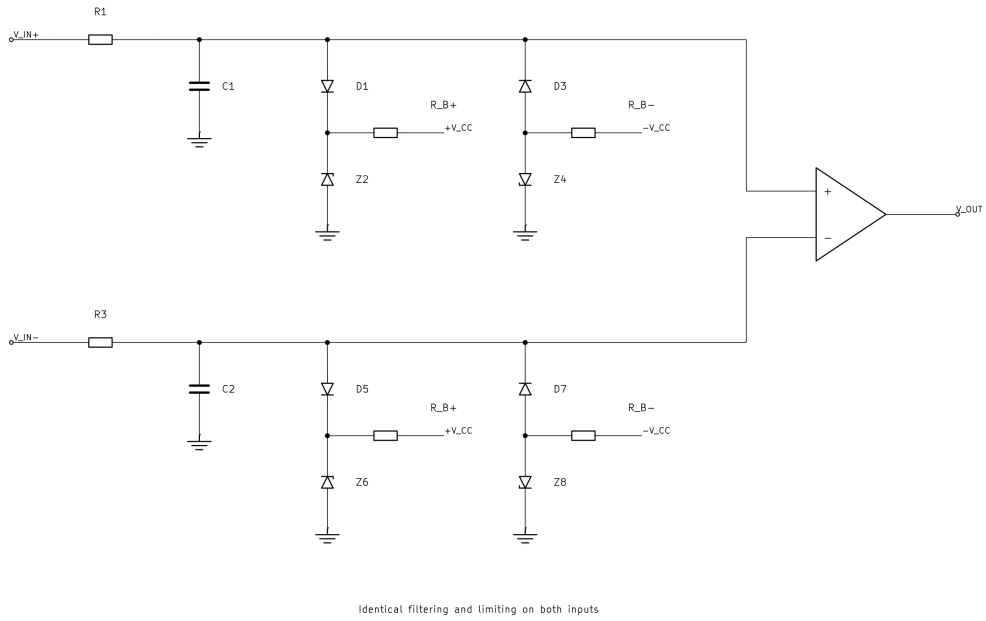


Figure 49. Matched bipolar input-limiting network ahead of the differential stage.

A practical limiter uses fast, low-leakage diodes connected to pre-biased Zener reference nodes. The positive and negative conduction thresholds are approximately

$$V_{CL+} \simeq V_{Z+} + V_{F+}, \quad V_{CL-} \simeq -\left(V_{Z-} + V_{F-}\right). \tag{119}$$

The input series resistor limits clamp current. The low-leakage protection-diode capacitance appears in parallel with the intentional shunt capacitance and is small relative to the nanofarad-scale capacitor shown. The two input paths remain symmetrical so that the limiter does not degrade differential balance.

5.9.Safety isolation and leakage current

An isolation barrier has finite impedance, so an isolated supply does not by itself remove every leakage path between a remote source and earth. Leakage current is determined by the complete return path, including the barrier impedance and any additional earth connection.

6.Analogue filtering and anti-aliasing

The filter sequence is developed from frequency-selective behaviour and Bode construction to disturbance separation, anti-aliasing, response-family selection, and the active low-pass and high-pass stages used by the conditioning channel.

6.1.Purpose of filtering in a measurement chain

A filter is a frequency-selective system: it applies a different gain and phase shift to different sinusoidal components of a signal. That selectivity can be used in several ways. A filter can retain the part of a spectrum that carries useful information, suppress out-of-band noise, divide a broadband signal into independently processed bands, support spectral-energy measurements, or compensate the non-flat response of another part of the signal chain. When filters are combined with amplifiers, attenuators, and summing stages, the resulting network can deliberately shape the overall frequency response.

This last point is important. Frequency dependence is not intrinsically desirable or undesirable. In one system it is an imperfection to be corrected; in another it is the mechanism used to correct an imperfection elsewhere. Equalisation is a direct example: the equaliser applies the inverse or partial inverse of an unwanted spectral weighting so that the complete chain reproduces the original information more faithfully.

The filter therefore does not create information. It redistributes the amplitudes and phases of components already present. Any reduction of unwanted content must be weighed against distortion of the wanted signal.

6.2.Transfer function, sinusoidal testing, and notation

A linear time-invariant filter multiplies each sinusoidal component by a complex frequency response. Its magnitude changes the component amplitude and its argument changes the phase. With input and output spectra denoted by $S_i(f)$ and $S_u(f)$, the relation is

$$S_u(f) = H(f)S_i(f), \quad H(f) = K(f)e^{j\phi(f)}. \tag{120}$$

The diagrams use $K(f)$ for the amplitude response. A sinusoidal test at frequency f measures

$$K(f) = |H(f)| = \frac{V_{\text{out}}(f)}{V_{\text{in}}(f)}, \quad G_{\text{dB}}(f) = 20\log_{10}K(f). \tag{121}$$

Input and output must use the same amplitude convention, such as RMS or peak-to-peak voltage. A value of one means unchanged amplitude; zero means complete suppression in the ideal model. A negative decibel value means attenuation, not a reversal of polarity. Phase is a separate part of the response.

For a signal containing several sinusoids, the output is the sum of the individually filtered components:

$$v_{\text{in}}(t) = \sum_k A_k\cos(2\pi f_k t + \theta_k), \quad v_{\text{out}}(t) = \sum_k A_k K(f_k)\cos(2\pi f_k t + \theta_k + \phi(f_k)). \tag{122}$$

This component-by-component description connects the ideal spectrum examples to the later measurements of waveform deformation. Preserving amplitudes alone is insufficient when the relative timing of the components matters.

6.3.Ideal frequency-selective models

6.3.1.Ideal low-pass filter

An ideal unity-gain low-pass retains frequencies below its cutoff f_t and rejects frequencies above it. Figure 50 relates this rule to the filter block and its rectangular magnitude response.

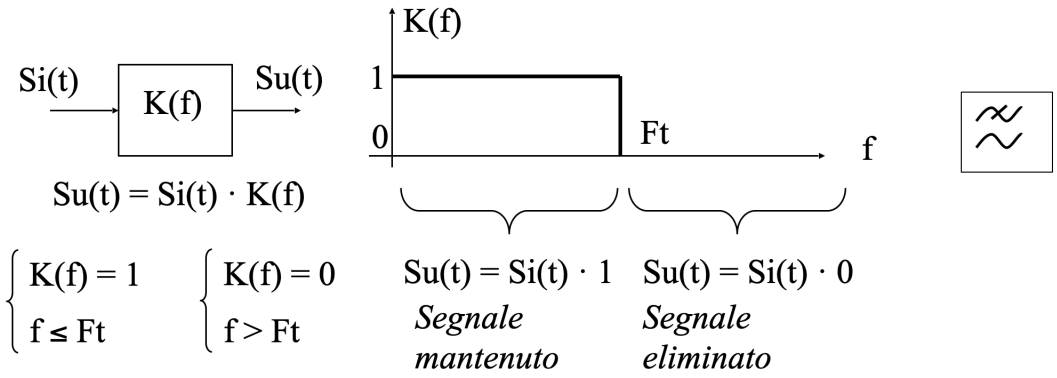


Figure 50. Ideal low-pass block and rectangular magnitude response.

$$K_{\mathrm{LP,id}}(f) = \begin{cases} 1, & 0 \le f \le f_t, \\ 0, & f > f_t . \end{cases} \tag{123}$$

The six-line example in Figure 51 applies that response to each input component. The components f_1, f_2 and f_3 lie below the cutoff and retain their amplitudes. The higher components f_4, f_5 and f_6 are removed. The blue annotation identifies retained components and the red annotation identifies rejected components.

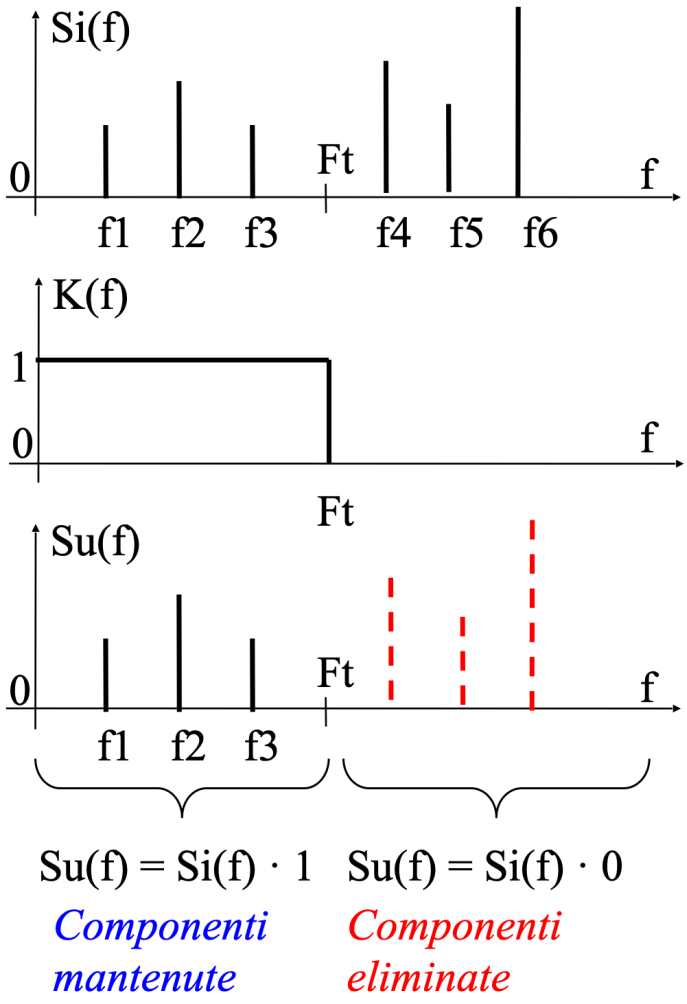


Figure 51. Component-by-component action of an ideal low-pass filter.

6.3.2.Ideal high-pass filter

The high-pass response reverses the selection: low frequencies are rejected and high frequencies pass. The block and ideal magnitude response are shown in Figure 52.

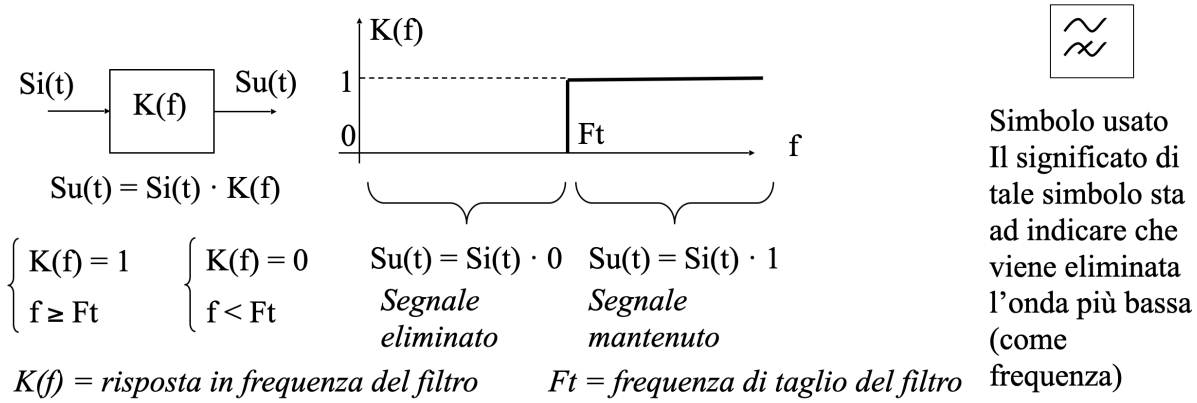


Figure 52. Ideal high-pass block and rectangular magnitude response.

$$K_{\mathrm{HP,id}}(f) = \begin{cases} 0, & 0 \le f < f_t, \\ 1, & f \ge f_t. \end{cases} \tag{124}$$

In Figure 53, f_1, f_2 and f_3 are below the cutoff and disappear from the output, while f_4, f_5 and f_6 remain. A high-pass therefore removes a DC component as well as sufficiently slow variations. Its cutoff must lie below the lowest useful signal frequency if those variations are part of the measurement.

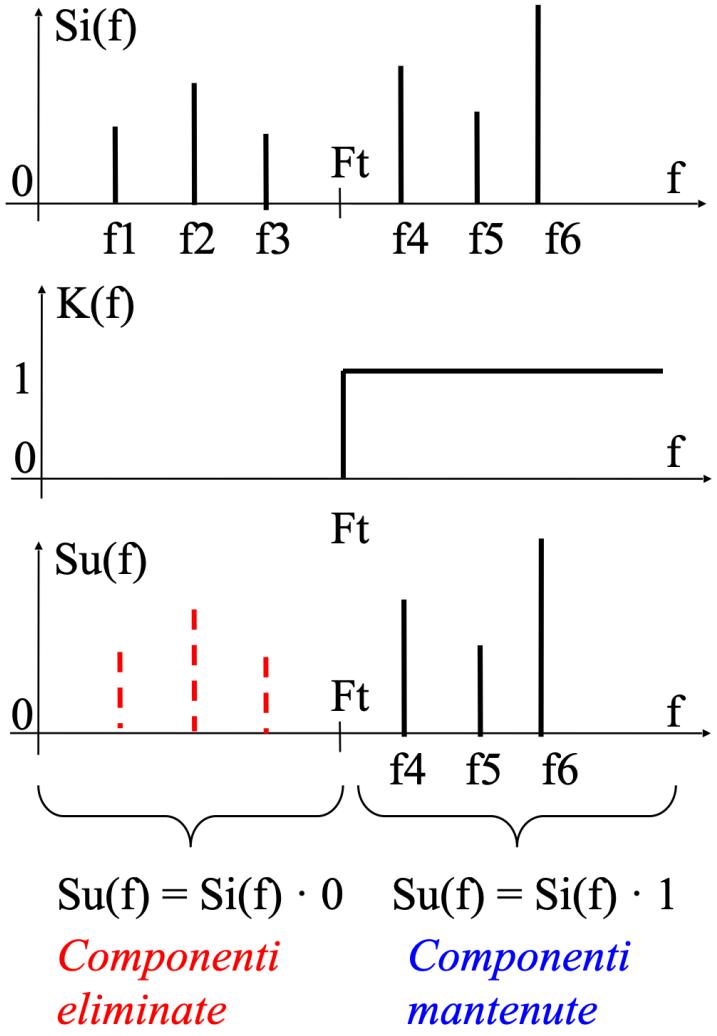


Figure 53. Component-by-component action of an ideal high-pass filter.

6.3.3.Ideal band-pass response by cascade

A band-pass retains an interval bounded by a lower cutoff f_L and an upper cutoff f_H, with $f_L < f_H$. Figure 54 shows the low-pass response $K_B(f)$, the high-pass response $K_A(f)$ and their common passband. In the diagram, $F_t(A) = f_L$ and $F_t(B) = f_H$.

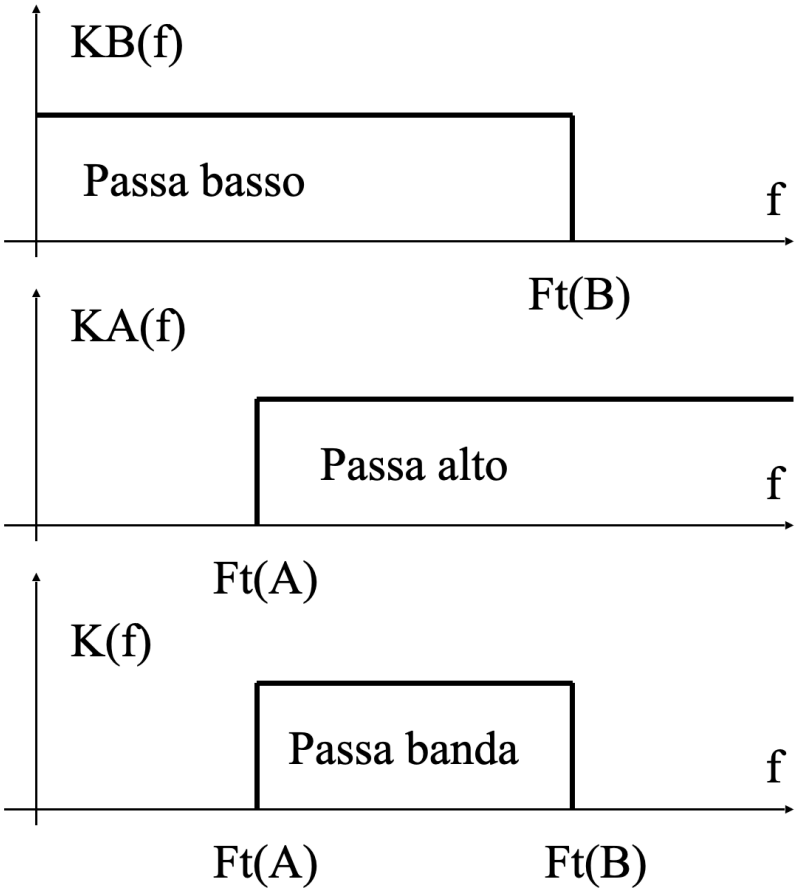


Figure 54. Overlap of ideal low-pass and high-pass responses forming a band-pass.

Cascading the blocks makes every component pass through both selections. Figure 55 shows the intermediate spectrum $S_x(f)$ after the low-pass and the final spectrum after the high-pass.

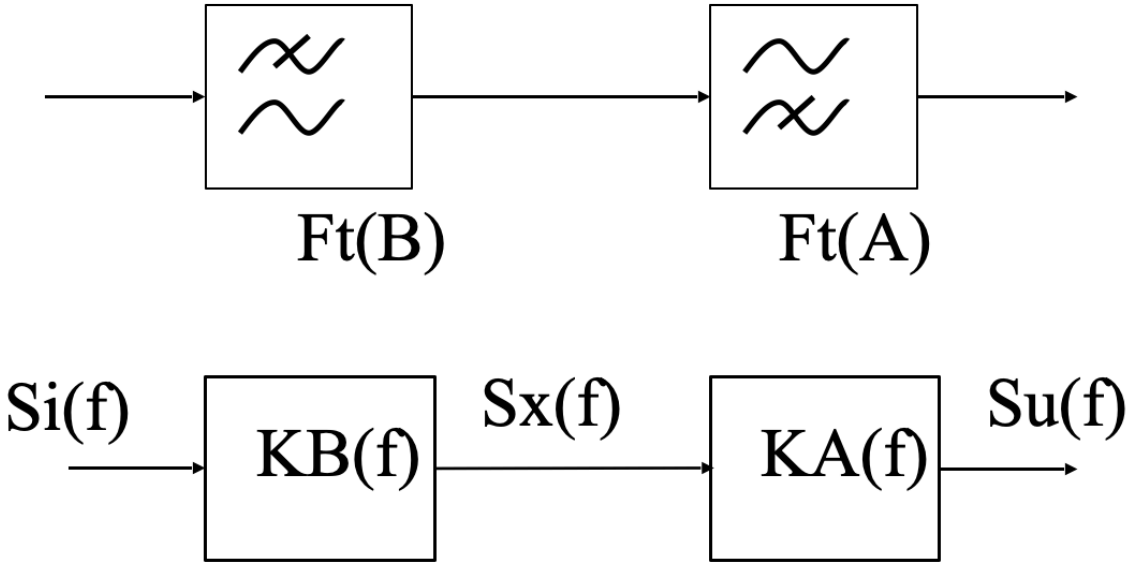


Figure 55. Low-pass followed by high-pass, with the intermediate spectrum identified.

$$S_x(f) = S_i(f)K_B(f), \quad S_u(f) = S_x(f)K_A(f) = S_i(f)K_B(f)K_A(f). \tag{125}$$

$$K_{\mathrm{BP,id}}(f) = \begin{cases} 1, & f_L \le f \le f_H, \\ 0, & \text{otherwise}. \end{cases} \tag{126}$$

The example in Figure 56 places f_2, f_3 and f_4 inside the common passband. The first component is below the lower cutoff; the fifth and sixth are above the upper cutoff. Both spectral tails are rejected.

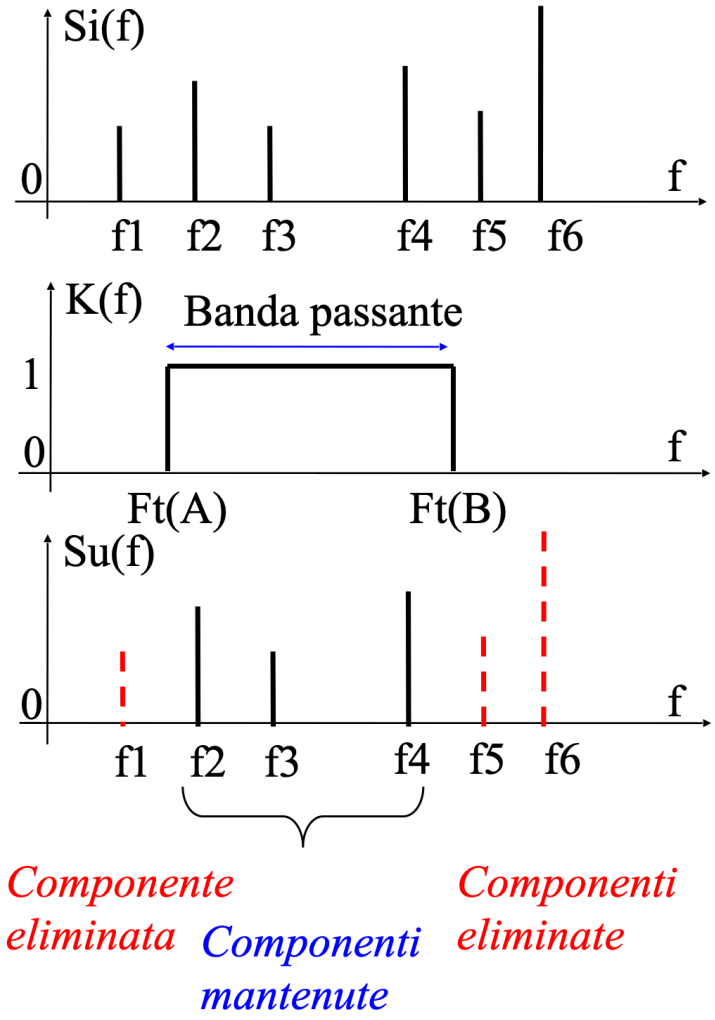


Figure 56. Intermediate spectral components retained by an ideal band-pass filter.

The order can be reversed in the ideal linear model, as shown in Figure 57. The intermediate spectrum then contains the high-pass output, denoted $S_y(f)$, but the final response is unchanged because the two transfer functions multiply.

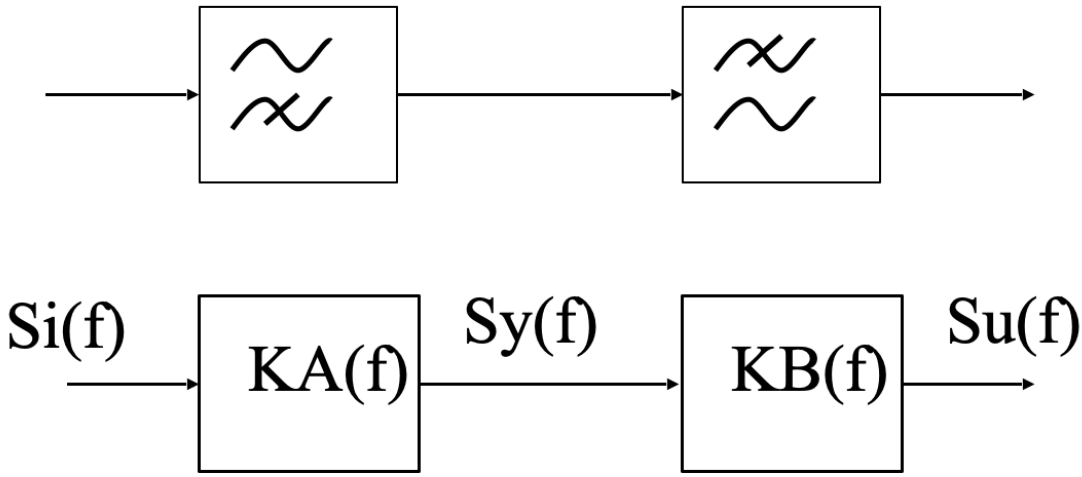


Figure 57. Reversed high-pass and low-pass order with a different intermediate spectrum.

$$S_y(f) = S_i(f)K_A(f), \quad S_u(f) = S_y(f)K_B(f) = S_i(f)K_A(f)K_B(f). \tag{127}$$

This interchange is valid only when loading does not alter either stage and both remain linear. The intermediate signal can differ substantially between the two orders. Headroom, overload recovery and the noise introduced by each real stage can therefore determine the practical order even when the small-signal product is identical.

6.3.4.Ideal band-stop response by parallel summation

A band-stop network uses parallel branches instead of a cascade. Figure 58 sends the same input to a low-pass branch and a high-pass branch, then adds their outputs. The sum retains the low- and high-frequency tails.

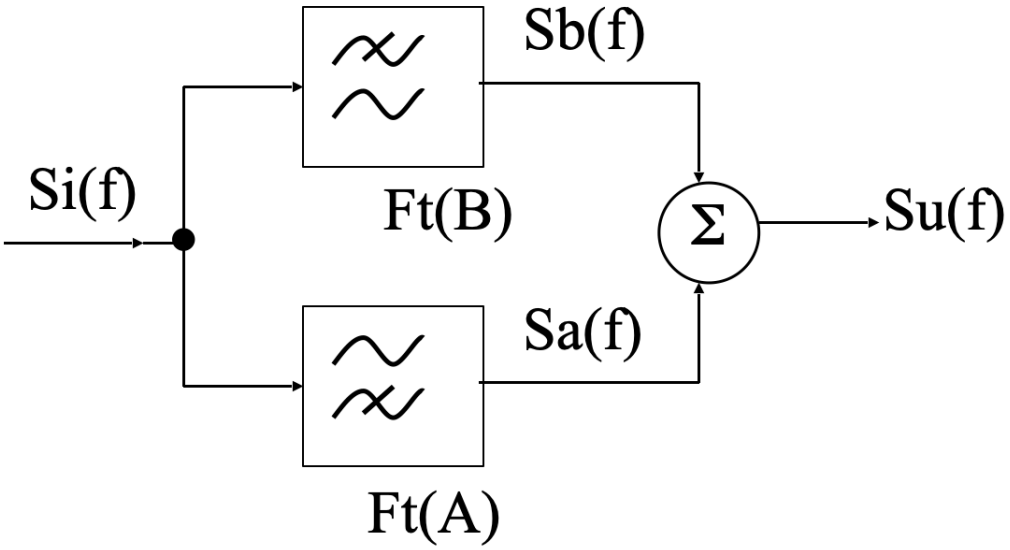


Figure 58. Parallel low-pass and high-pass branches feeding a summing node.

$$S_u(f) = S_b(f) + S_a(f) = S_i(f)\left[H_B(f) + H_A(f)\right]. \tag{128}$$

For the ideal masks in Figure 59, the low-pass cutoff is below the high-pass cutoff. Here $F_t(B) = f_L$ and $F_t(A) = f_H$, the opposite ordering of the labelled cutoffs from the band-pass construction. Both branches reject frequencies strictly between these limits.

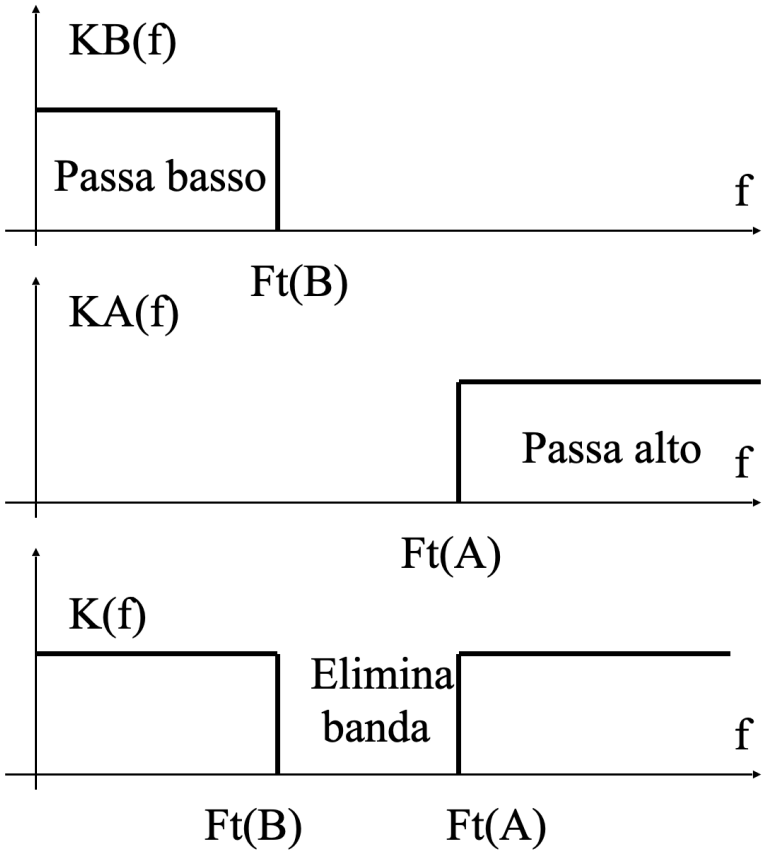


Figure 59. Two outer passbands separated by the rejected interval of an ideal band-stop.

$$K_{\mathrm{BS,id}}(f) = \begin{cases} 1, & f \le f_L \text{ or } f \ge f_H, \\ 0, & f_L < f < f_H . \end{cases} \tag{129}$$

For real branches the complex responses must be added, including their phase. Adding magnitude curves or decibel values does not describe a parallel summer. Passband flatness and cancellation around the rejected interval depend on the gains, phases and transition regions of both branches.

6.3.5.Why the ideal brick-wall model is not physically realisable

The rectangular masks define which frequencies should be retained; they are not finite-order analogue circuits. A real filter has a finite transition band, residual stopband transmission and frequency-dependent phase. The assignment of a single ideal boundary frequency does not alter that practical distinction.

6.4.Cascaded systems and addition in decibels

For cascaded stages whose individual responses are not changed by loading, the complete transfer function is the product of the stage responses. Figure 60 groups two, three and four first-order sections to show how the products are built.

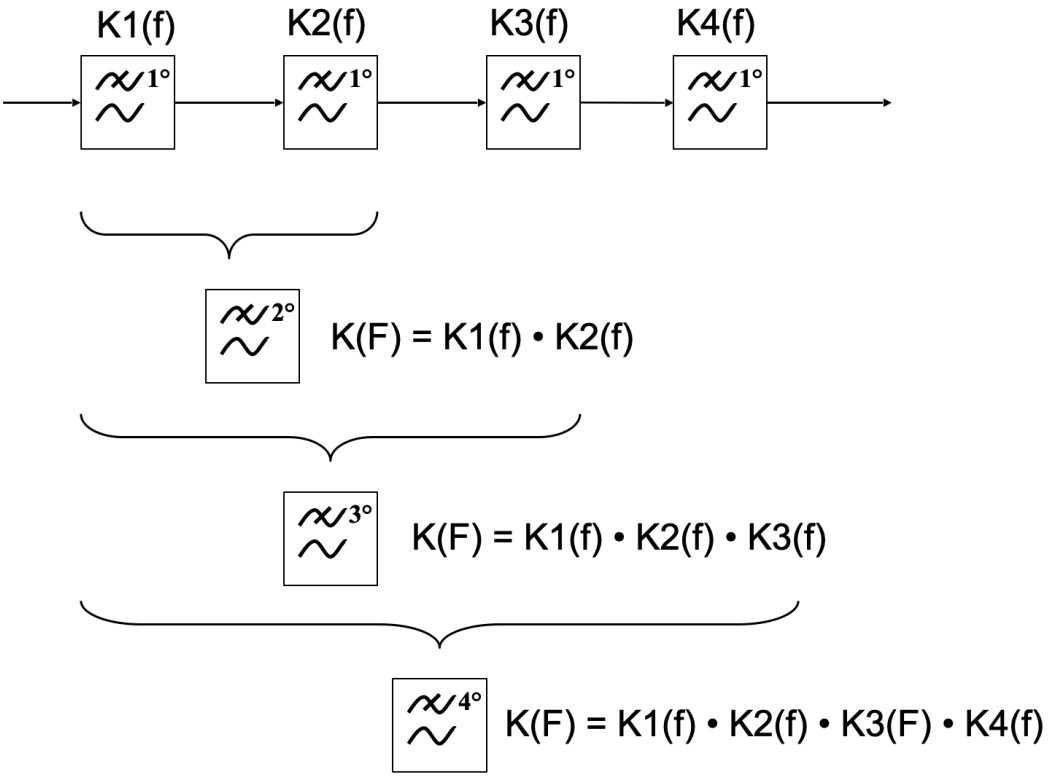


Figure 60. Products of first-order stage responses forming higher-order cascades.

$$H_{\text{tot}}(f) = \prod_{i=1}^{M} H_i(f), \quad |H_{\text{tot}}(f)| = \prod_{i=1}^{M} |H_i(f)|. \tag{130}$$

$$G_{\text{tot,dB}}(f) = \sum_{i=1}^{M} 20\log_{10}|H_i(f)|. \tag{131}$$

The phase shifts also add. Each added first-order low-pass pole contributes an eventual magnitude slope of minus 20 dB per decade. Order counts the poles of the resulting transfer function after any cancellations; the number of boxes alone is not enough if the boxes contain different orders or interact electrically.

6.4.1.Decibel reference values

For a voltage ratio $A_v = V_{\text{out}}/V_{\text{in}}$:

Table 2. Decibel reference values.

A_v	Gain	Interpretation
2	+6.02 dB	voltage doubled
4	+12.04 dB	voltage quadrupled
10	+20 dB	one voltage decade of gain
1	0 dB	unity gain
0.5	-6.02 dB	voltage halved
0.1	-20 dB	one voltage decade of attenuation
0.001	-60 dB	voltage divided by 1000

The cutoff of a conventional first-order low-pass or high-pass is not the half-amplitude point. At cutoff the amplitude is $1/\sqrt{2} \approx 0.707$, corresponding to approximately -3 dB. A value of approximately -6 dB corresponds to half amplitude.

6.5.Logarithmic frequency axes and Bode plots

A logarithmic frequency axis gives equal distances to equal frequency ratios. An octave doubles frequency; a decade multiplies it by ten. One decade contains approximately 3.322 octaves. A first-order stopband slope of 20 dB per decade is therefore approximately 6.02 dB per octave.

A Bode magnitude plot expresses $20\log_{10}|H(f)|$ against logarithmic frequency. A first-order low-pass asymptote is flat below its pole frequency and falls above it; the first-order high-pass asymptote rises below its pole frequency and is flat above it. Asymptotes simplify the arithmetic, while the true response rounds the corner.

6.6.Real first-order low-pass and high-pass behaviour

For an unloaded RC section, or for a buffered section whose loading is negligible, the unity-passband transfer functions are

$$H_{\mathrm{LP}}(s) = \frac{1}{1 + sRC}, \quad H_{\mathrm{HP}}(s) = \frac{sRC}{1 + sRC}, \quad f_t = \frac{1}{2\pi RC}. \tag{132}$$

Writing $x = f/f_t$ gives the magnitude responses

$$|H_{\mathrm{LP}}| = \frac{1}{\sqrt{1 + x^2}}, \quad |H_{\mathrm{HP}}| = \frac{x}{\sqrt{1 + x^2}}. \tag{133}$$

At the corner, both magnitudes are $1/\sqrt{2}$, approximately 0.707 of the passband amplitude or -3.01 dB. The low-pass has a phase of -45 degrees there; the high-pass has +45 degrees under the stated transfer-function convention. Figure 61 shows the straight-line low-pass construction with a -6 dB-per-octave stopband slope.

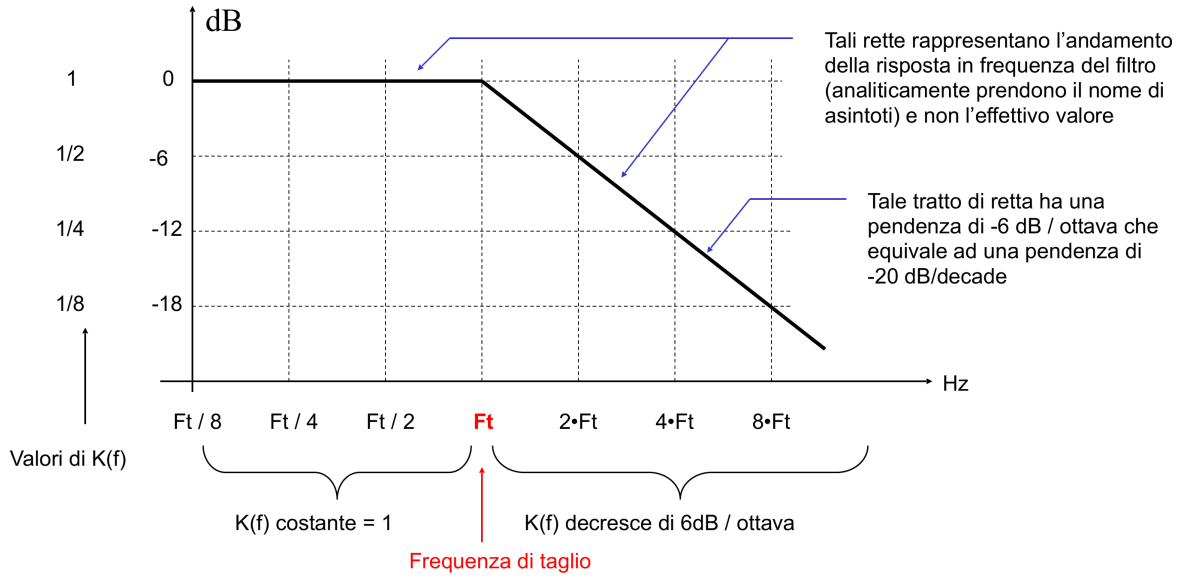


Figure 61. First-order low-pass asymptotic Bode construction.

Figure 62 compares the approximate real curve with the asymptotes and applies it to an input spectrum. The component at the corner is reduced from 1 V to about 0.7 V. Components above the corner remain present at reduced amplitudes; they do not vanish as in the ideal mask. The illustrated 0.5 V and 0.2 V outputs are rounded graphical estimates, not exact RC values.

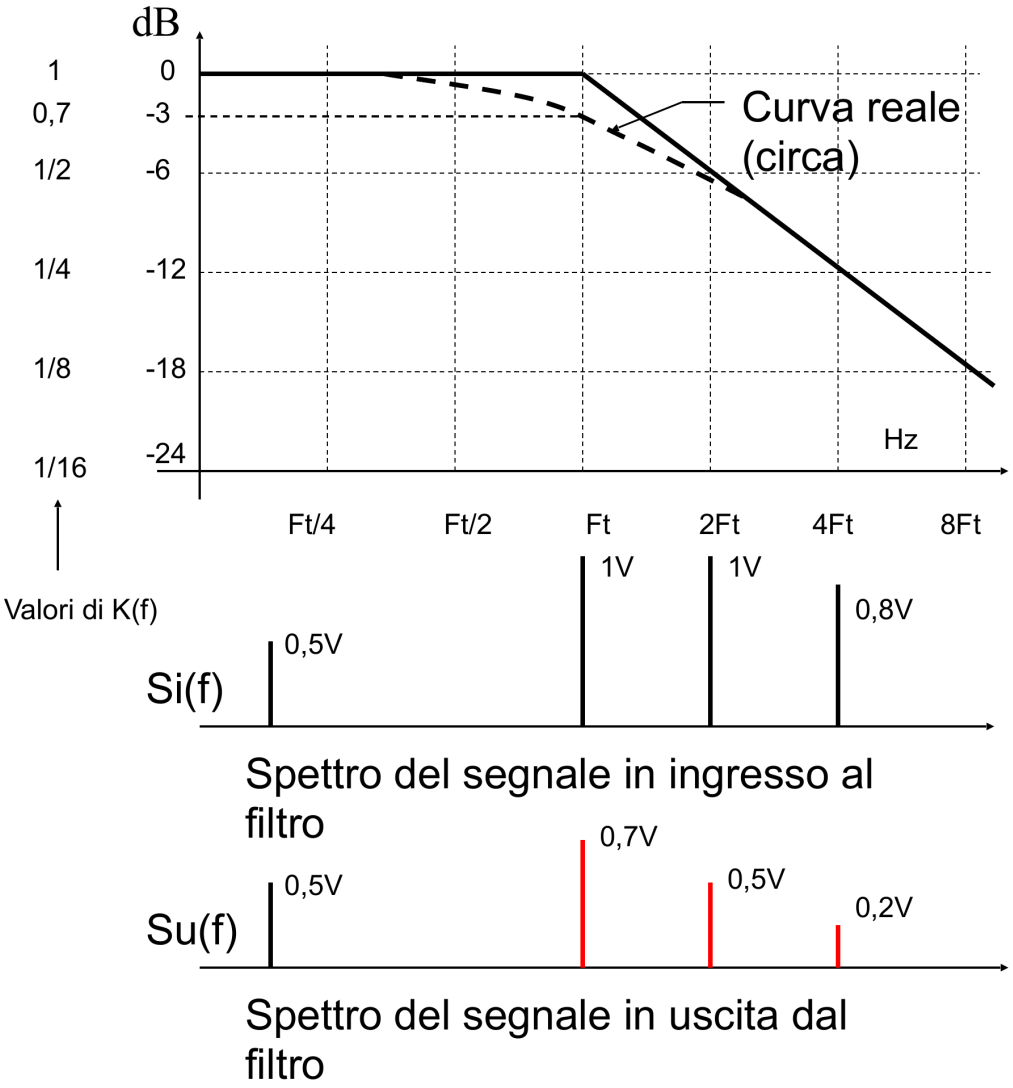


Figure 62. Real first-order low-pass transition and its action on input spectral components.

6.7.Filter order and selectivity

Figure 63 compares the asymptotic slopes of first- through fourth-order low-pass responses: approximately -6, -12, -18 and -24 dB per octave. A higher order supplies greater rejection sufficiently far into the stopband, but the transition shape also depends on the chosen pole alignment.

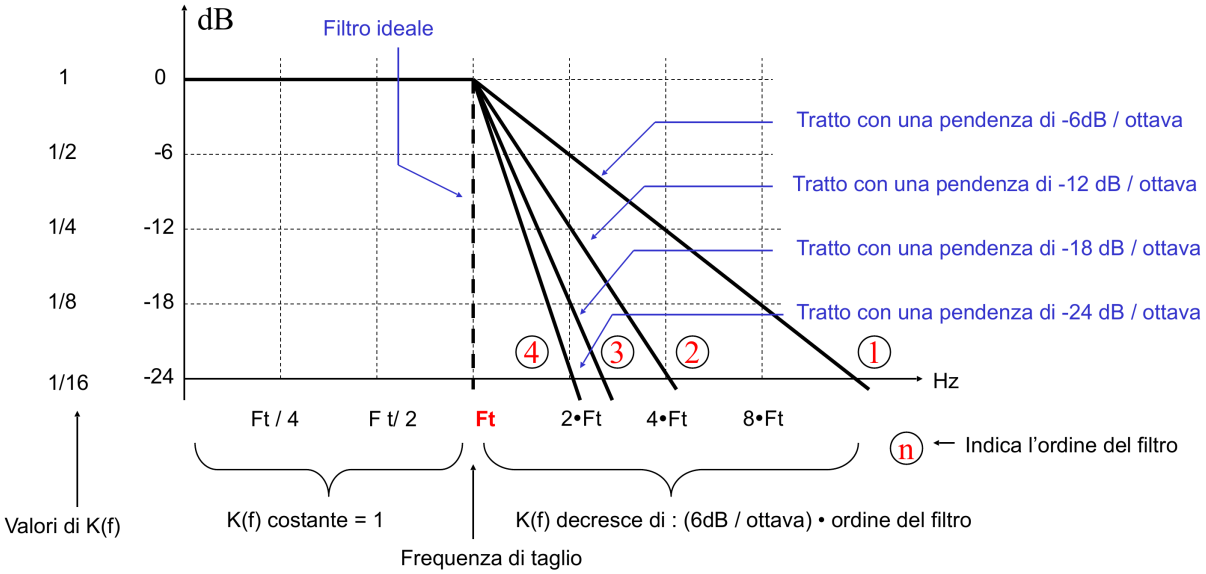


Figure 63. First- through fourth-order low-pass response family and asymptotic stop-band slopes.

Cascading identical first-order sections does not preserve a common -3 dB cutoff. Each section contributes -3.01 dB at its own corner, so two identical sections produce -6.02 dB there. A specified Butterworth, Chebyshev or Bessel response therefore requires its own pole frequencies and damping, rather than an arbitrary stack of identical cells.

6.8.Reading cascaded Bode plots

The following examples combine the gains of individual blocks at each frequency. Their red resultant curves are asymptotic sums. The exact response rounds every corner and may not reach the apparent plateau when the transition bands overlap.

6.8.1.First-order band-pass with gain

Figure 64 combines a first-order high-pass at 250 Hz, a first-order low-pass at 1 kHz and a gain of four. The amplifier adds about 12 dB at every frequency. Below 250 Hz the high-pass contribution rises at 6 dB per octave; above 1 kHz the low-pass contribution falls at the same rate.

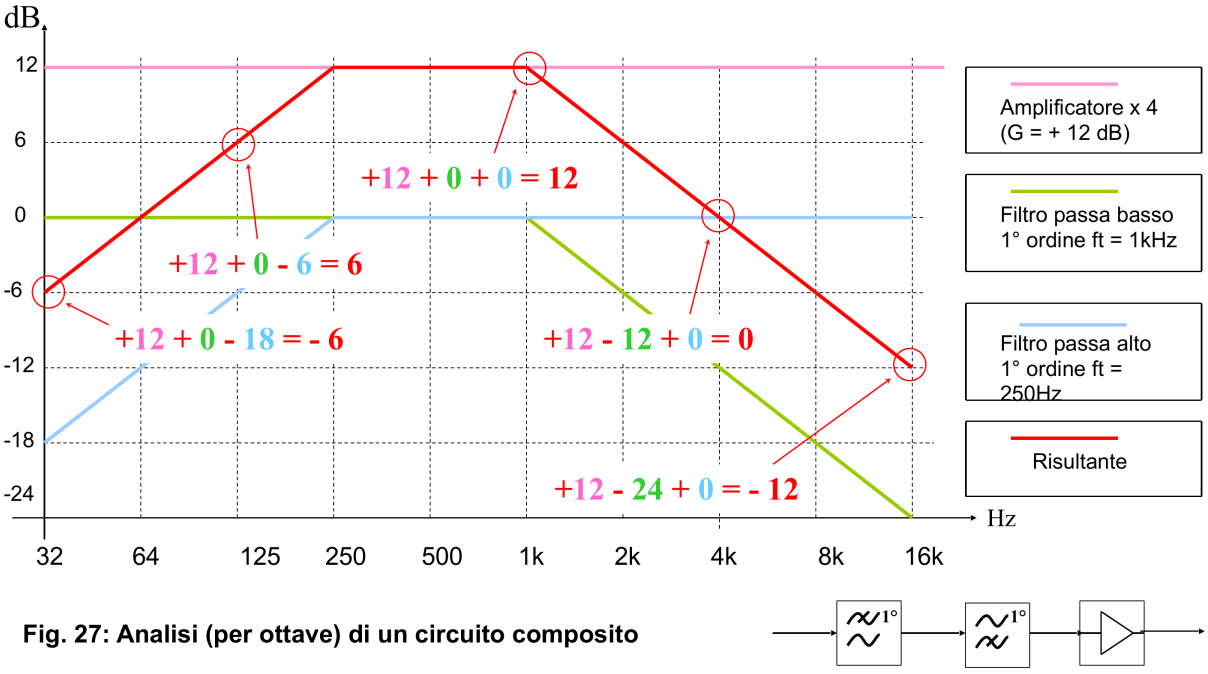


Fig. 27: Analisi (per ottave) di un circuito composito

Figure 64. Asymptotic sum of a 250 Hz first-order high-pass, a 1 kHz first-order low-pass and gain four.

For example, the asymptotic sum is +6 dB at 125 Hz, +12 dB at 1 kHz, 0 dB at 4 kHz and -12 dB at 16 kHz. These values come from adding the individual decibel contributions, not from reading the exact rounded transfer function.

6.8.2.Different orders on the two skirts

In Figure 65, the upper filter becomes a second-order low-pass at 4 kHz. The lower first-order high-pass remains at 250 Hz, and the amplifier gain remains four. The lower skirt therefore rises at 6 dB per octave while the upper skirt falls at 12 dB per octave.

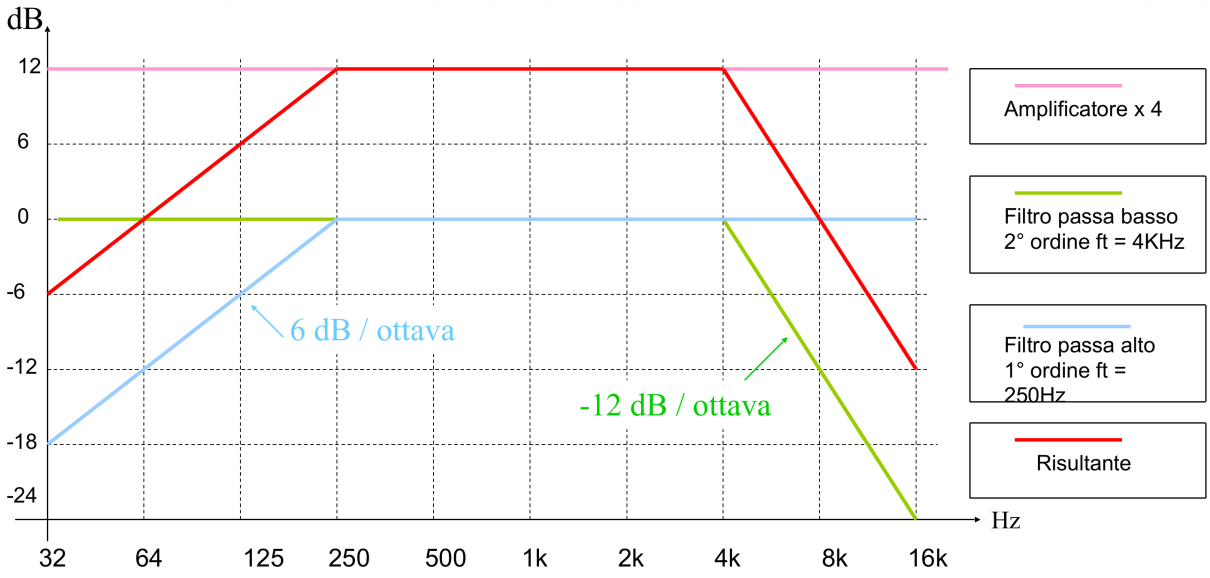


Fig. 28: Analisi (per ottave) di un circuito composito

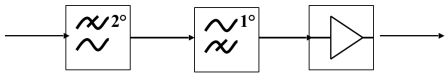


Figure 65. Asymmetric band-pass skirts from a first-order high-pass and a second-order low-pass with gain four.

Replacing the gain-of-four amplifier by a divide-by-four attenuator lowers the entire magnitude response by approximately 24 dB without changing the filter poles. Gain sets the vertical position; the filters set the transition frequencies and asymptotic slopes.

6.8.3.A six-decade example

A second-order high-pass at 0.1 Hz, a third-order low-pass at 100 kHz and a gain of ten produce a nominal +20 dB passband. Their lower and upper asymptotic skirts have slopes of +40 and -60 dB per decade. Decades are convenient here because the band spans six orders of magnitude.

6.8.4.Staggered first-order transition frequencies

Figure 66 cascades first-order low-pass sections with corners at 2, 4 and 8 kHz. The total asymptotic slope changes from zero to -6, -12 and finally -18 dB per octave as successive poles contribute.

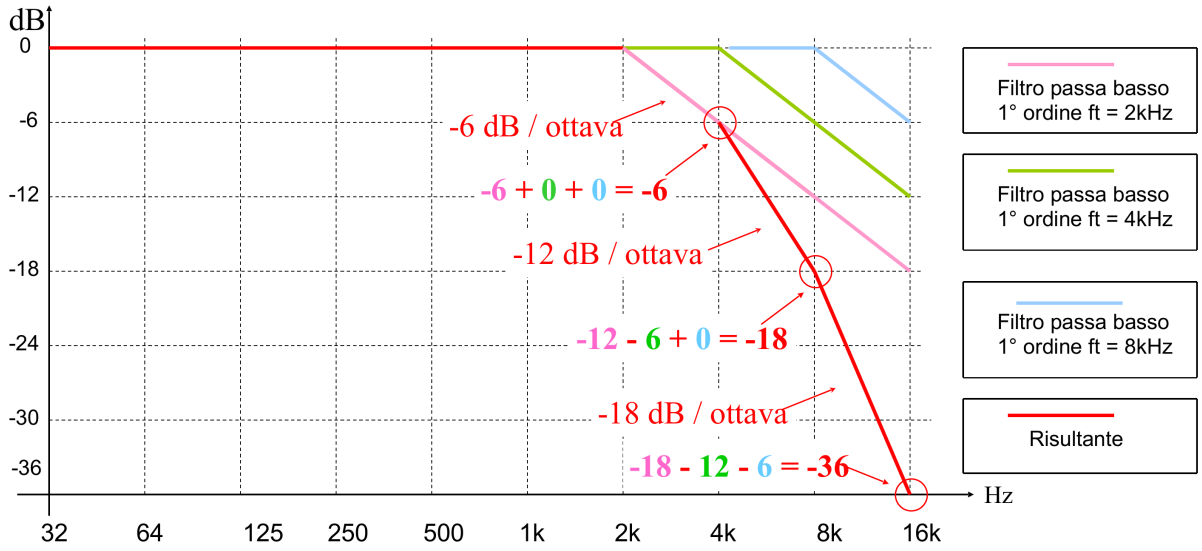


Fig. 31: Analisi (per ottave) di un circuito composito

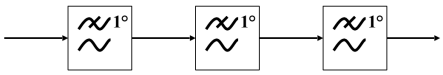


Figure 66. Cascaded first-order sections with staggered transition frequencies and cumulative stop-band slope.

At 4 kHz, the first section contributes -6 dB. At 8 kHz, the first two contribute -12 and -6 dB, giving -18 dB in total. At 16 kHz, the three contributions are -18, -12 and -6 dB, giving -36 dB. The rounded exact response differs near each corner, but the calculation explains the cumulative attenuation.

6.9.Filtering before analogue-to-digital conversion

A low-pass can separate wanted and unwanted content only when their spectra allow it. Figure 67 distinguishes well-separated bands, closely spaced bands and overlapping bands. Modest order can be sufficient in the first case; the second demands a sharper transition. In the overlap region of the third case, a frequency-selective filter attenuates wanted and unwanted components together.

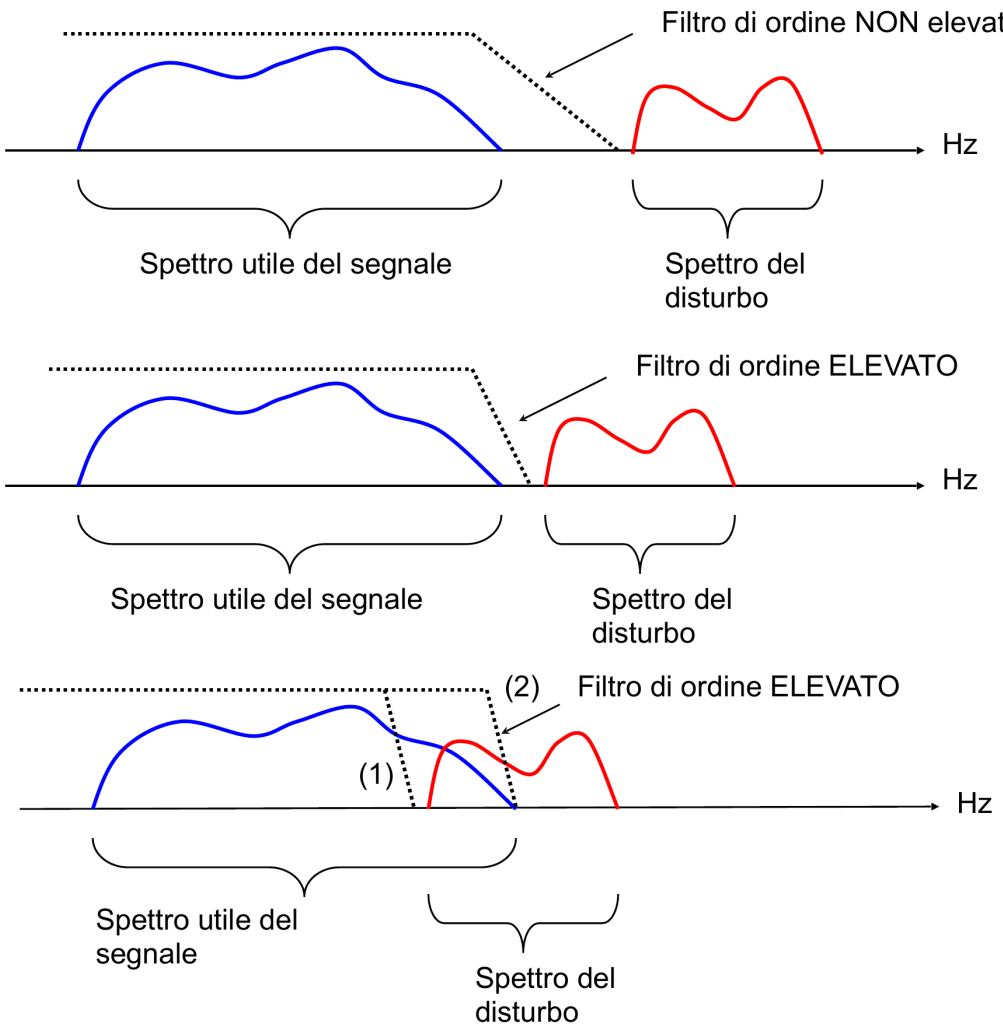


Figure 67. Three spectral-separation cases for useful and disturbing components.

The analogue filter must also attenuate components that would fold into the useful band during sampling. Figure 68 follows the complete sequence from transducer and amplifier through analogue low-pass filtering, sampling, sample-and-hold and A/D conversion. The red annotation states the purpose of the low-pass: to band-limit the signal before it is sampled.

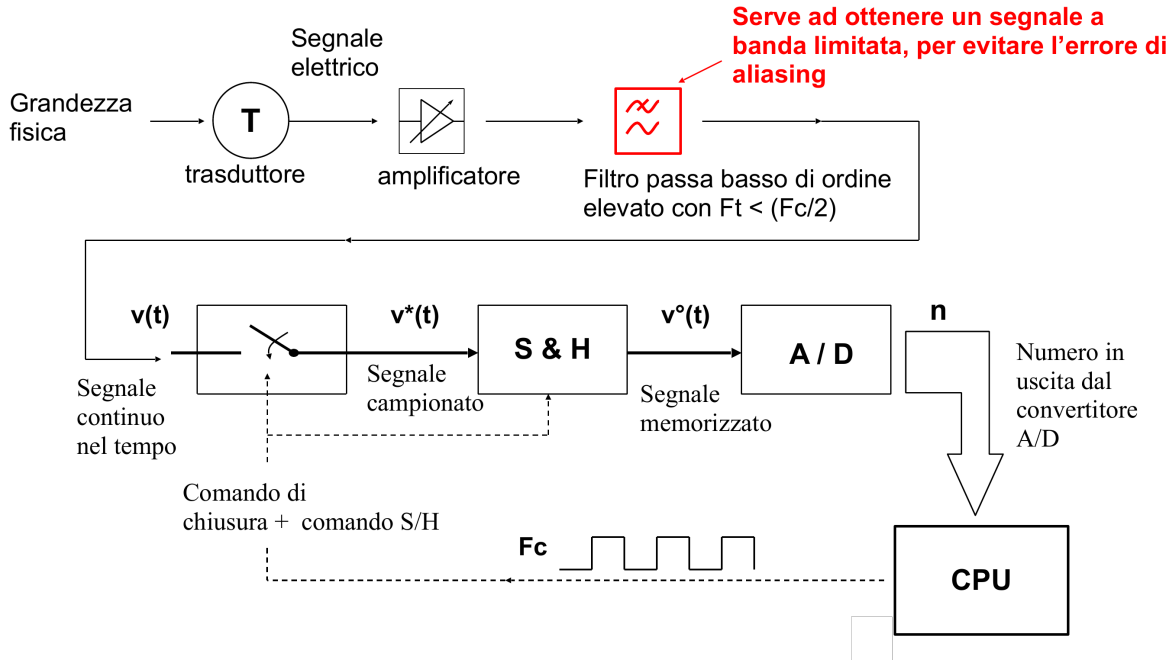


Figure 68. Signal chain from transducer through analogue anti-alias filtering to sampling and numerical conversion.

The diagram uses F_c for the sampling frequency, denoted f_s here, and F_t for the filter transition frequency. The simplified condition $f_t < f_s/2$ leaves room for a transition band, but it is not by itself an anti-alias specification. A real design must provide sufficient attenuation at every frequency that can alias into the measurement band, accounting for the largest expected unwanted input.

Sampling can map a component at f to an indistinguishable baseband component at $|f - nf_s|$ for an integer n. Once that overlap has occurred, subsequent digital filtering cannot distinguish it from a wanted component at the same sampled frequency. The sample-and-hold stabilises each sample for conversion; it does not replace the preceding analogue anti-alias filter.

6.10.Fifth-order active low-pass implementation

The fifth-order low-pass circuit in Figure 69 combines five equal series resistors, five capacitors and two unity-gain FET-input followers. The active RC feedback paths form Sallen-Key sections. The complete pole pattern is determined jointly by the network; the unbuffered RC portions must not be treated as independent sections with arbitrary corner frequencies.

The complete fifth-order circuit is shown in Figure 69.

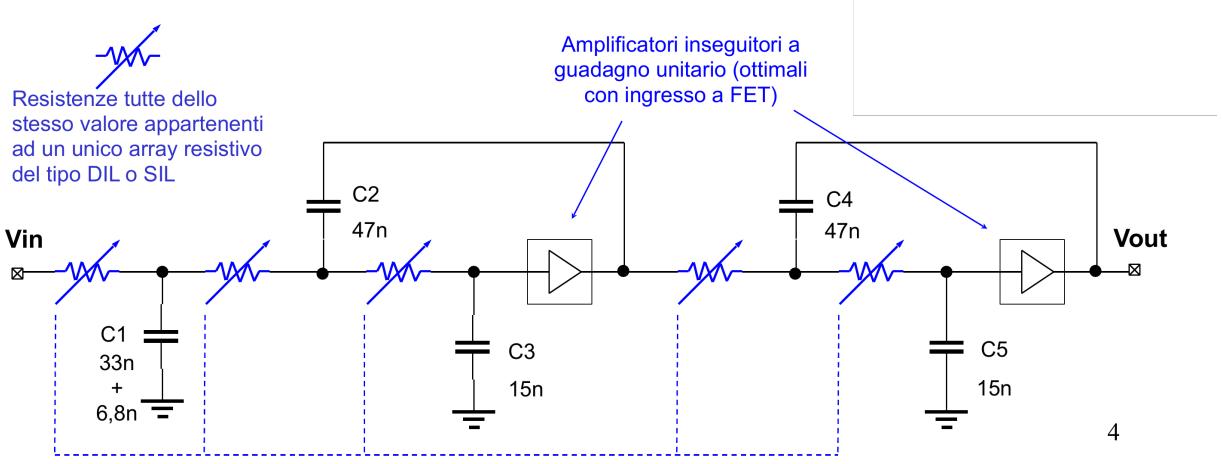


Figure 69. Fifth-order active low-pass network with five reactive elements and buffered sections.

For the displayed Bessel implementation, the capacitors are labelled

$$C_1 = 33\ \text{nF} + 6.8\ \text{nF},\quad C_2 = C_4 = 47\ \text{nF},\quad C_3 = C_5 = 15\ \text{nF}\,. \tag{134}$$

The indicated values are the nearest 5% commercial approximations to the intended theoretical values. Butterworth or Chebyshev behaviour can be obtained by changing the capacitor values while retaining the same general circuit and common resistor array.

The DC gain is unity because the amplifiers operate as followers. The cutoff is adjusted through the common resistor value; discrete settings separated by half an octave, one octave or one decade are sufficient for the intended module. Changing all five resistances together preserves the chosen response shape while translating its frequency range.

The reason for selecting the Bessel version in the proposed conditioning path is its transient behaviour. The displayed comparison shows practically no overshoot for the Bessel response, whereas the Butterworth and Chebyshev alternatives show increasing overshoot and ringing as the transition becomes more aggressive.

6.11.Fifth-order Bessel, Butterworth, and Chebyshev comparison

The SIGLENT captures dated 24 July 2026 compare the measured frequency and time responses of the Bessel, Butterworth and Chebyshev low-pass configurations. Their transition regions lie around 1 kHz. The purpose is to establish how much interference each configuration rejects and how faithfully it preserves the timing and shape of a transient.

Measured magnitude and phase

Figures 70–72 use the same logarithmic frequency span, 100 Hz to 10 kHz. Magenta is the measured amplitude response on the left axis; green is phase on the right axis. Bessel starts to lose passband amplitude earlier, but its transition is gentler, so it attenuates less than Butterworth and Chebyshev at the same frequency beyond the transition. Earlier passband droop and weaker stopband rejection are different aspects of that trade-off.

The Bessel measurement in Figure 70 shows the gradual transition. Its relatively smooth phase evolution is consistent with the Bessel design objective of nearly constant group delay over the useful passband. This is the feature that helps keep the surviving spectral components of a transient aligned in time.

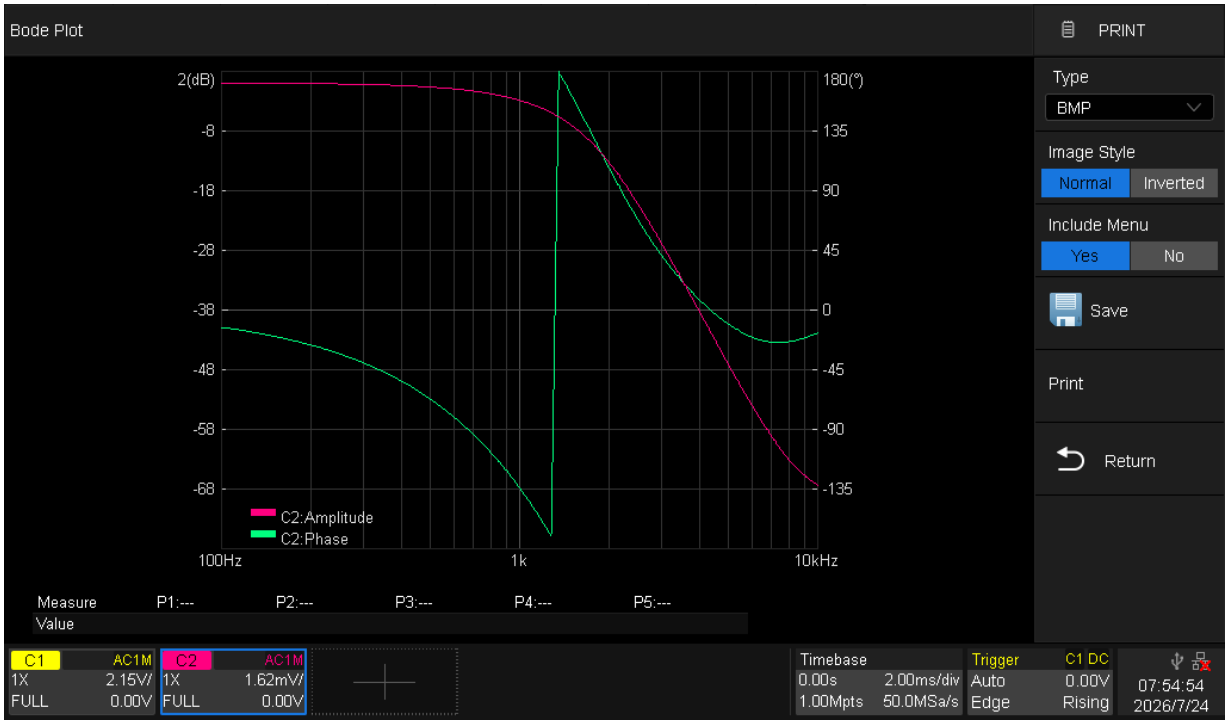


Figure 70. Measured Bessel Bode plot: magnitude in magenta and wrapped phase in green.

Butterworth holds a flatter passband and then falls more steeply, as shown in Figure 71. Its phase changes more rapidly around the transition. The improved magnitude selectivity therefore comes with a less uniform delay across the frequencies that form a fast edge.

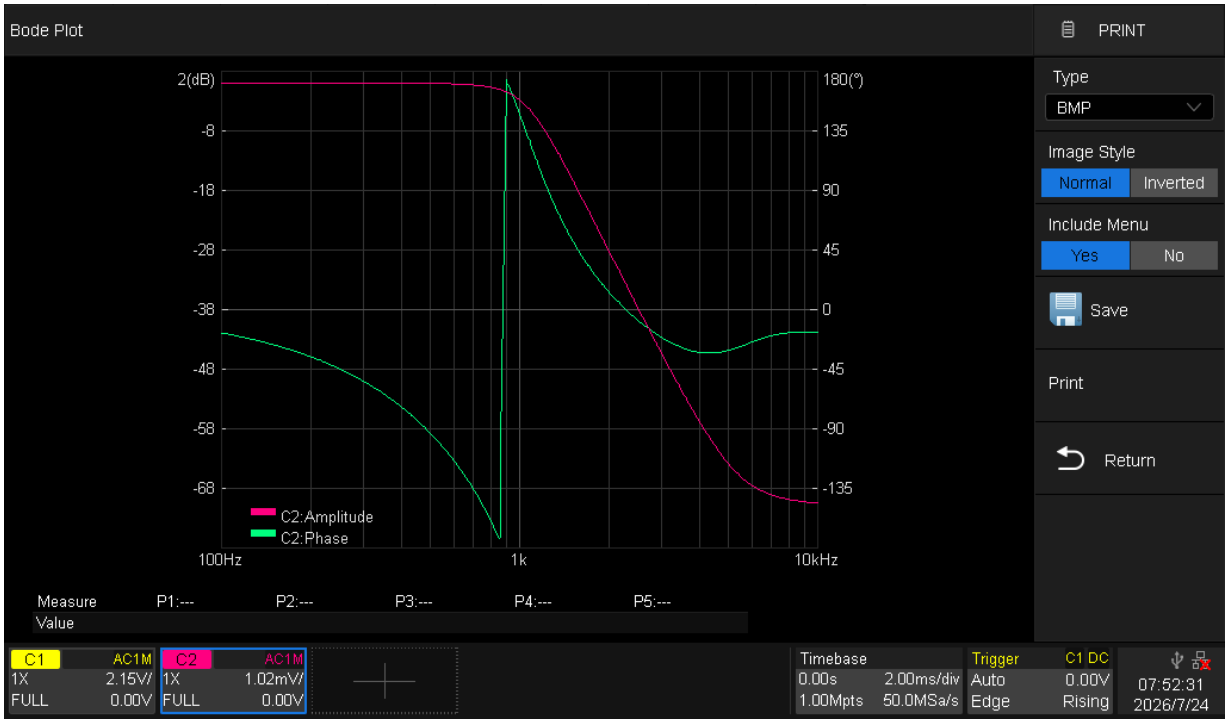


Figure 71. Measured Butterworth Bode plot on the same frequency and amplitude scales.

Chebyshev gives the strongest rejection immediately beyond the transition in Figure 72, with small passband ripple and still more concentrated phase rotation. At 2 kHz, the displayed gain is approximately −13 dB for Bessel, −28 dB for Butterworth and −39 dB for Chebyshev. These are coarse readings from the common graticules, not instrument cursor measurements. The extreme stopband traces should not be used to infer precise filter order or phase behaviour from these screenshots alone.

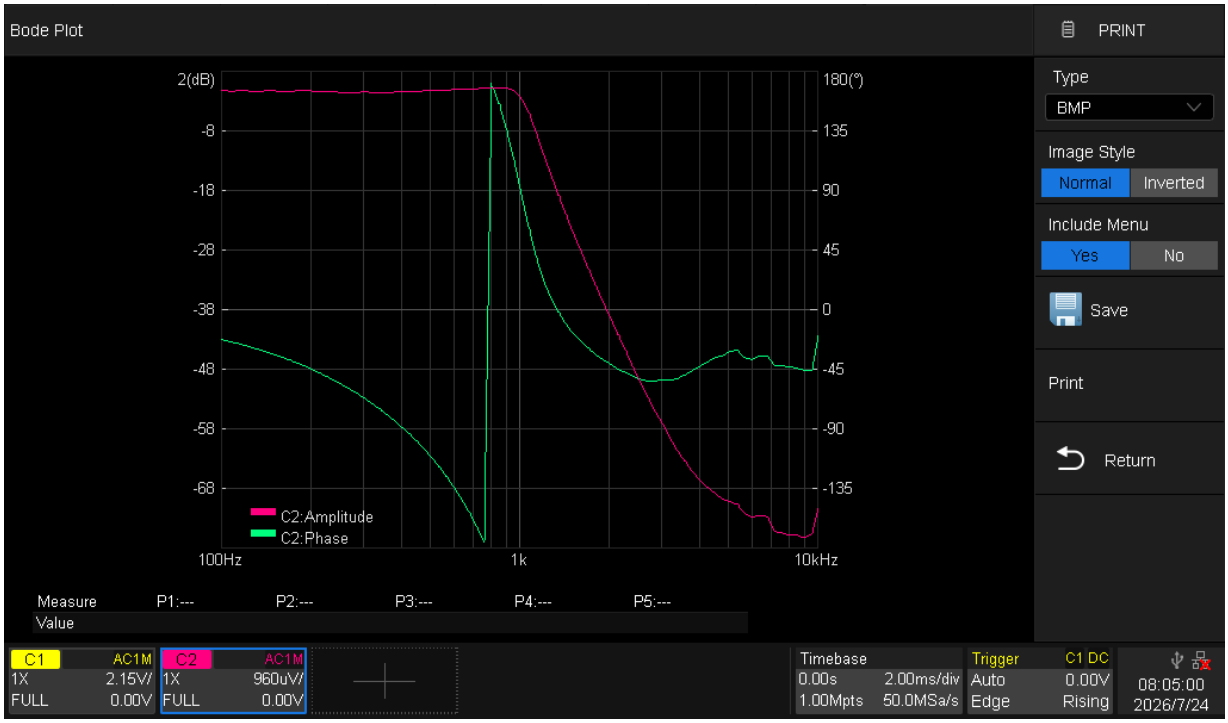


Figure 72. Measured Chebyshev Bode plot showing the sharpest transition of the three configurations.

The vertical jumps in the green traces are phase wrapping at the display boundary, not physical discontinuities in the filters. Linear phase means a nearly constant slope of unwrapped phase versus frequency on a linear frequency axis; it does not mean a straight line on this logarithmic display. Group delay is the negative slope of unwrapped phase with angular frequency. The screenshots show the family differences, but a numerical group-delay curve would require the underlying complex sweep data.

Measured edge delay and settling

Figures 73–75 show the rising edge of a 100 Hz square wave at 500 µs/div. C1 (yellow) is the input and C2 (magenta) is the output; both channels are at 5 V/div and are vertically offset for readability. Comparing the input transition with the output crossing halfway between its own settled levels gives approximate edge delays of 0.37 ms for Bessel, 0.55 ms for Butterworth and 0.65 ms for Chebyshev. These graticule estimates are edge delays, not measurements of group delay at a single frequency.

Bessel rounds the edge and delays it, but Figure 73 shows a rapid approach to the new level with very little visible overshoot. The output does not reproduce an infinitely sharp step: high-frequency content has been removed. Its advantage is that the transition remains well behaved after that bandwidth limitation.

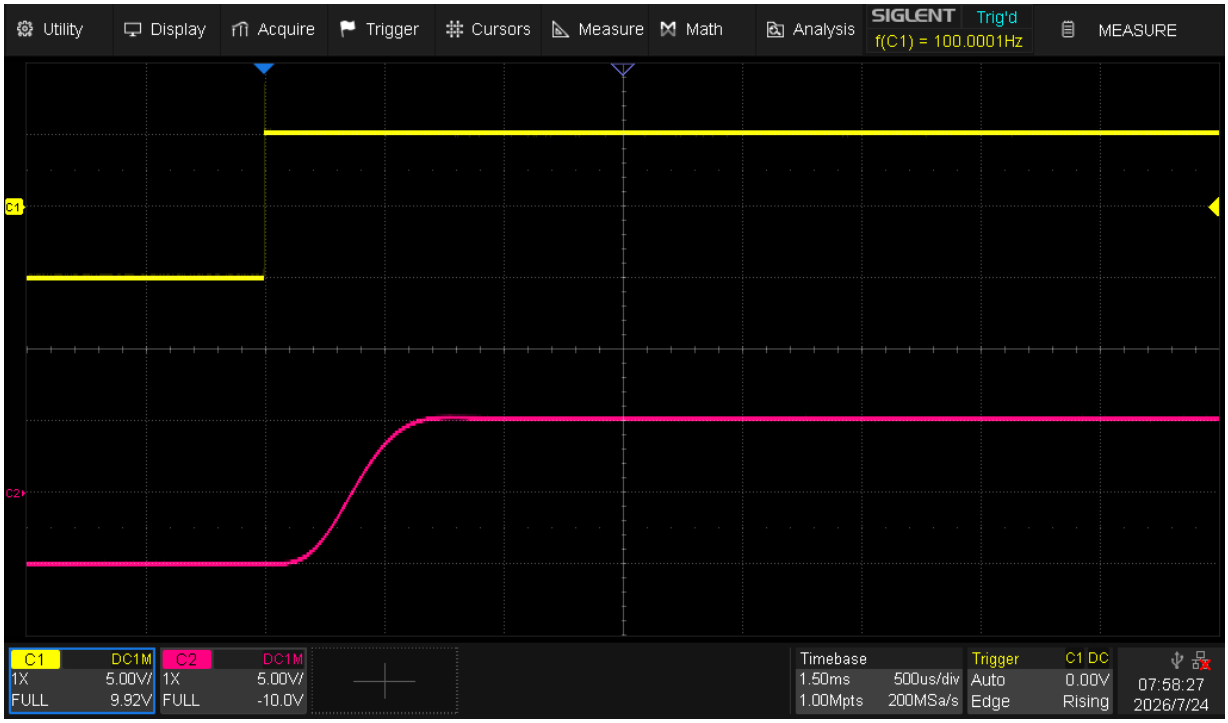


Figure 73. Measured Bessel edge response at 500 µs/div; input yellow, output magenta.

The Butterworth edge in Figure 74 arrives later and exceeds the final level by approximately 12% of the step height before returning through a small undershoot. That extra peak is created by the conditioning response; it is not present in the input. A time shift can align the main transition but cannot remove the overshoot and settling excursion.

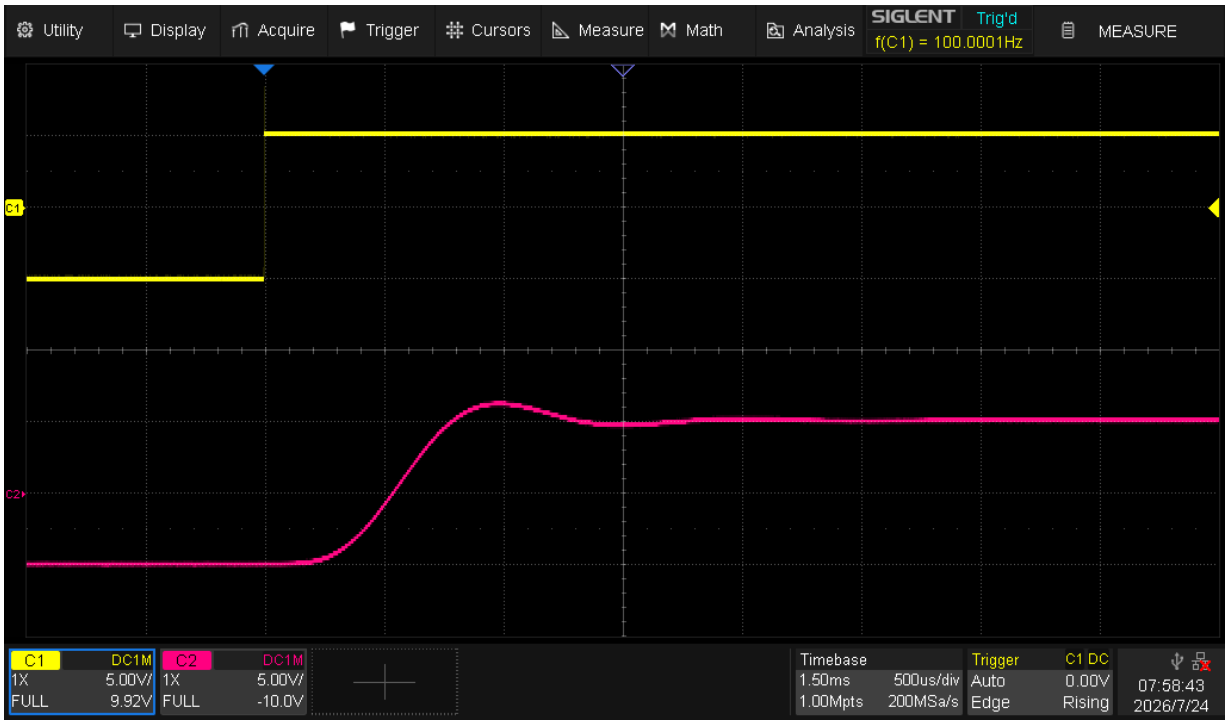


Figure 74. Measured Butterworth edge response at 500 µs/div, with overshoot and settling.

Chebyshev produces the latest transition and the most persistent ringing in Figure 75. Its first overshoot is also approximately 12% of the step height, but several alternating excursions remain after the input has already settled. The longer settling sequence is particularly damaging when adjacent transients or threshold events must be distinguished in time.

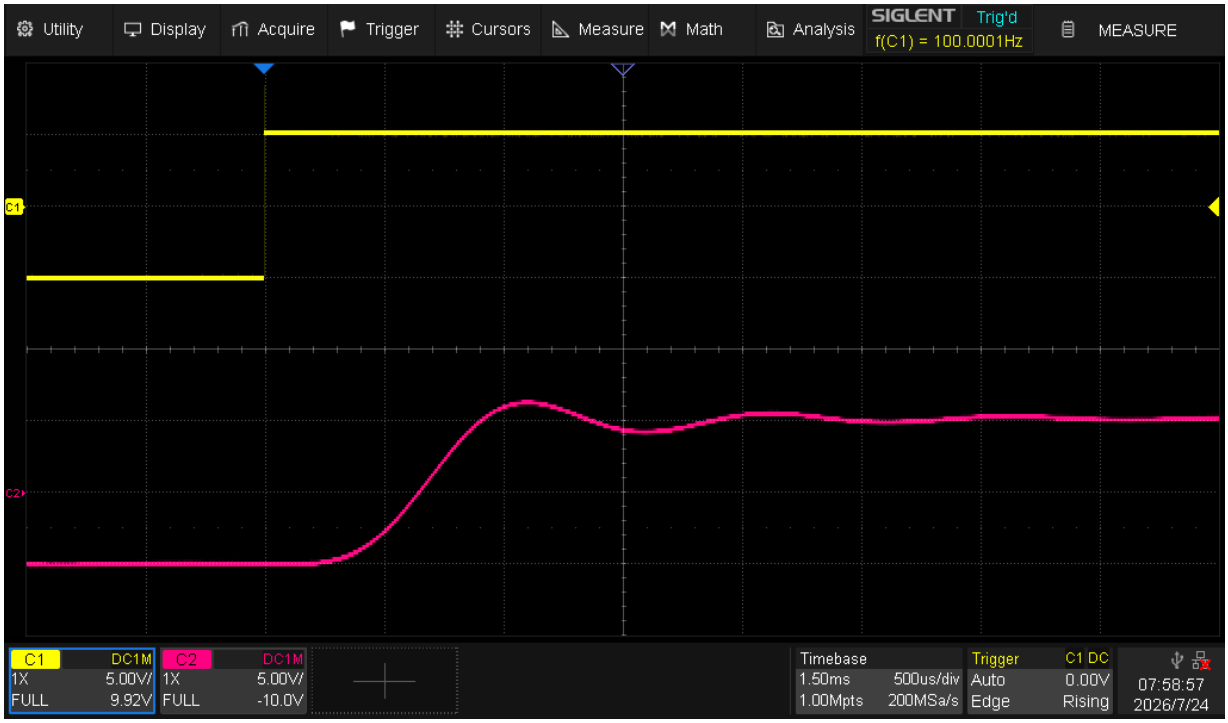


Figure 75. Measured Chebyshev edge response at 500 µs/div, with persistent ringing.

Measured distortion of a repeated waveform

Figures 76–78 use a 200 Hz square wave and a common timebase of 2 ms/div. C1 is at 2 V/div and C2 is at 5 V/div, with separate vertical offsets, so trace heights must not be compared as a gain measurement. Each half-cycle lasts 2.5 ms. The signal contains odd harmonics at 600 Hz, 1 kHz, 1.4 kHz and above as well as its 200 Hz fundamental; several shape-defining harmonics therefore lie near or beyond the filter transition.

In Figure 76, Bessel preserves a recognisable pulse train with rounded transitions and substantially flat plateaus. A delay remains, and the removed harmonics cannot be recovered simply by shifting the trace, but little additional ringing contaminates the retained waveform.

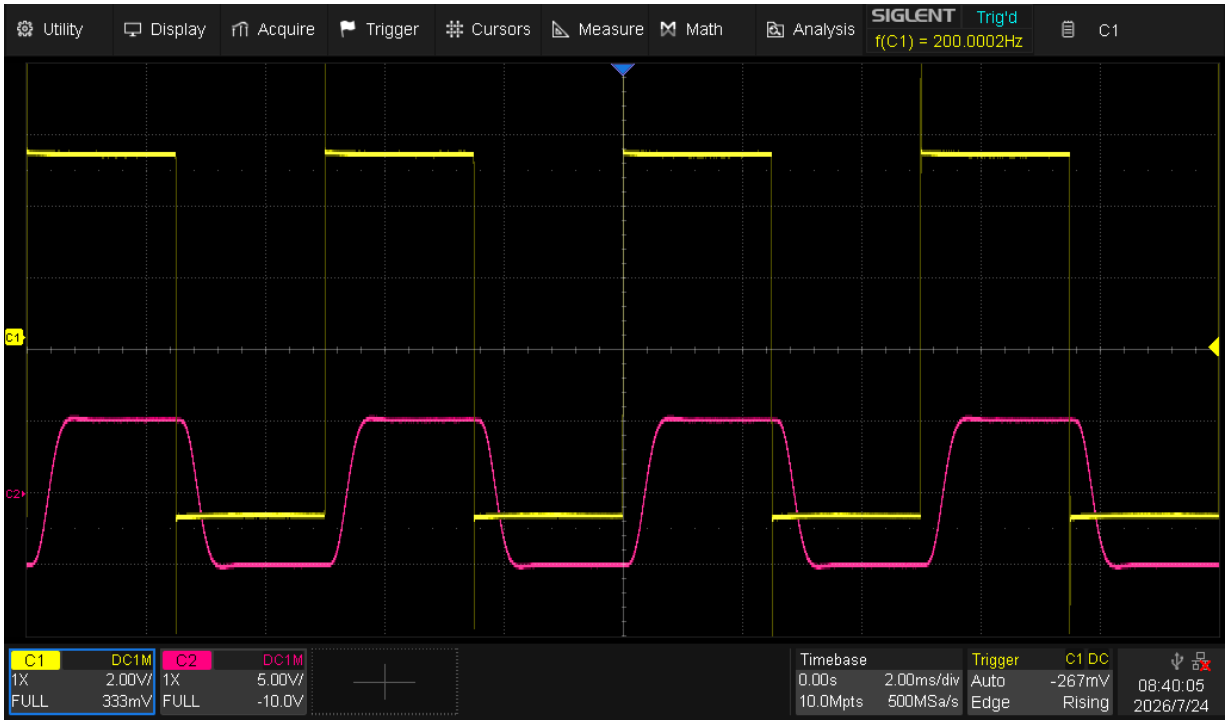


Figure 76. Measured Bessel output for a 200 Hz square wave at 2 ms/div.

In Figure 77, Butterworth changes the waveform throughout the repeated cycle. Overshoot and undershoot are the most visible symptoms, but altered harmonic amplitudes and relative phases also reshape the transitions and the signal between them. The output cannot be interpreted as a faithful time record merely by correcting its delay, even though the fundamental lies well below the filter transition.

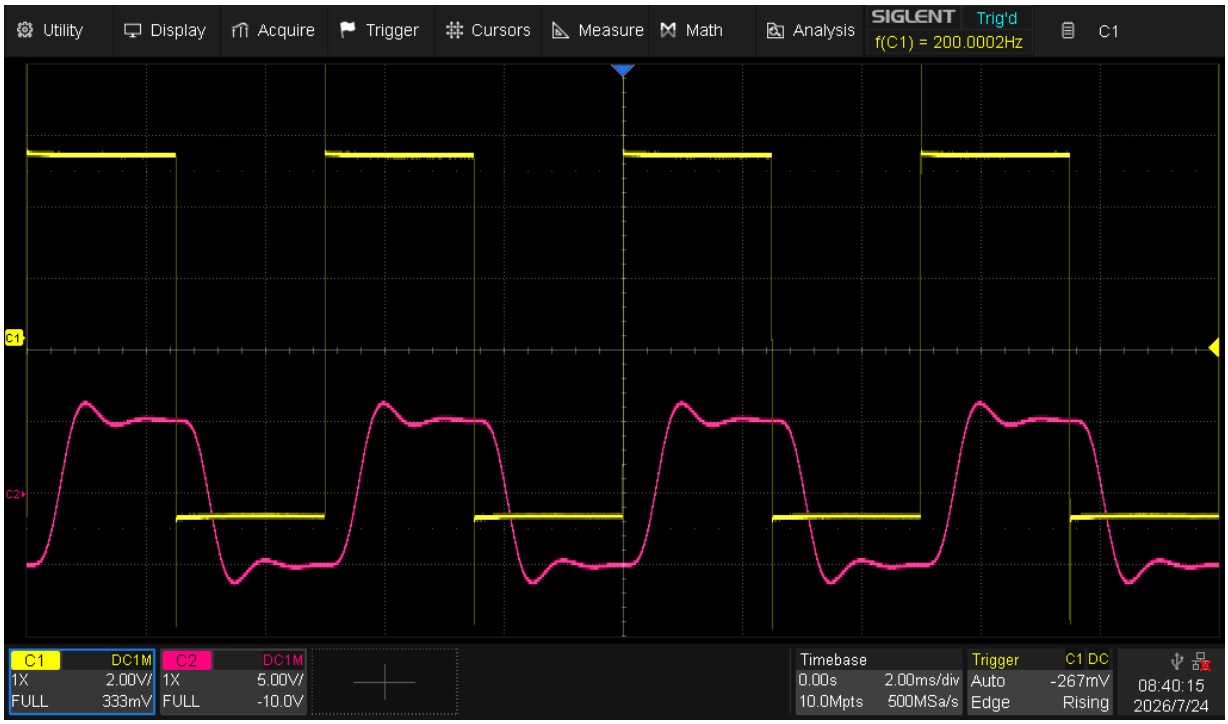


Figure 77. Measured Butterworth output for a 200 Hz square wave, with repeated overshoot and undershoot.

The Chebyshev output in Figure 78 is more severely deformed. Repeated ringing creates extra maxima and minima and changes the shape of the cycle. The square wave makes this response easy to see; the same filtering mechanism acts on continuously varying signals, where the responses to nearby changes can overlap.



Figure 78. Measured Chebyshev output for a 200 Hz square wave, with repeated ringing and waveform deformation.

Waveform fidelity and band strength measurements

For the measured configurations and tested signal, the Butterworth and Chebyshev outputs are unsuitable as delivered for faithful waveform measurement or temporal reconstruction. The failure concerns the waveform as a whole. Unequal harmonic gains and frequency-dependent delay alter how its components combine throughout the cycle; overshoot and ringing are visible consequences. The response to one change can persist into subsequent changes. This is not an error confined to edges or plateaus, and a time shift alone cannot reverse it.

Sharper frequency selection can be useful when the required result is signal strength in a defined band, such as RMS level, average power or integrated energy, rather than the waveform itself. Butterworth offers a flat passband; Chebyshev trades passband ripple for a sharper transition. Their bands are not ideal rectangular bins: power and energy measurements are weighted by the squared magnitude response, so gain, ripple and effective bandwidth must be accounted for. Short measurement windows can also be affected by delay and ringing.

Bessel is therefore the preferred response here for waveform-preserving acquisition. Its more uniform passband delay better preserves the relative timing of the retained harmonics, although attenuation and finite bandwidth still change the signal. Anti-alias rejection must be verified separately. This selection depends on signal bandwidth and required fidelity; Butterworth and Chebyshev are not restricted to energy measurements when other applications tolerate their amplitude and phase response.

6.12.Switchable first-/second-order high-pass implementation

The proposed high-pass stage contains two RC cells isolated by unity-gain FET-input followers. Its switches select three operating modes: direct bypass, one active RC cell for a first-order response, or both cells in cascade for a second-order response. Buffering prevents the second cell from materially loading the first and allows the switch selection to change order without changing the intended signal path.

The bypass, first-order and second-order routes are shown in Figure 79.

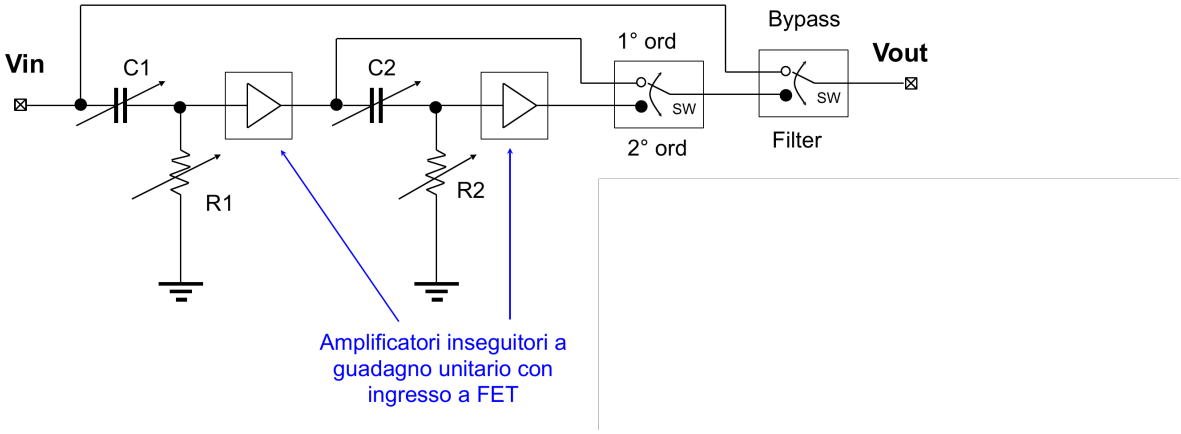


Figure 79. Switchable high-pass network providing first-order, second-order and bypass paths.

The implementation uses very large resistances, up to approximately 10 MΩ, so that low transition frequencies can be obtained with non-polarised polyester capacitors. This avoids the polarity constraint of an electrolytic capacitor when the signal can reverse direction. Selecting one or two cells changes both the low-frequency attenuation slope and the transient response; the implemented setting must be evaluated with its selected time constants.

This stage provides attenuation at the lower-frequency edge. The upper-band limitation required before sampling remains the function of the fifth-order low-pass stage.

7.Operational-amplifier foundations

The familiar closed-loop equations are valid only when negative feedback exists, the loop has adequate gain and stability, and every input and output node remains within the amplifier's real electrical limits.

7.1.Functional building blocks and the ideal operational amplifier

Three ideal functional blocks establish the operational-amplifier model:

- an amplifier with $V_y = G\,V_x$, $G > 1$, infinite input resistance, and zero output resistance, as shown in Figure 80;

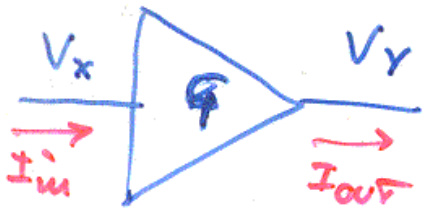


Figure 80. Gain block relating input voltage to output voltage through a constant factor.

- a subtractor with $V_3 = V_1 - V_2$ and no loading of either input, as shown in Figure 81;

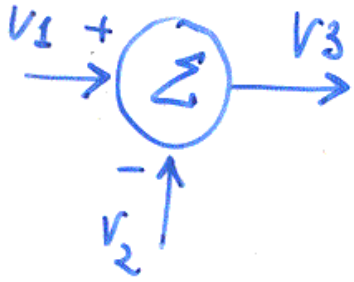


Figure 81. Signed summing node combining input voltages into one output voltage.

- an attenuator with $V_y = H\,V_x$, where $0 \le H \le 1$, as shown in Figure 82.

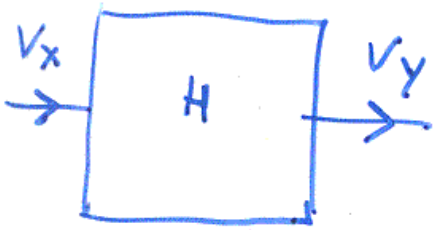


Figure 82. Attenuation block reducing an input voltage before a following stage.

Combining the subtractor and amplifier produces the ideal open-loop operational-amplifier law

$$V_{out} = A_{OL}(V_+ - V_-) = A_{OL} v_d\,. \tag{135}$$

In the ideal model,

$$A_{OL} \to \infty, \quad R_{IN} \to \infty, \quad R_{OUT} \to 0\,. \tag{136}$$

No current enters either input, and the output terminal acts as an ideal voltage source. These assumptions are not a description of the internal device. They are a controlled approximation used to analyse a circuit after negative feedback has forced the amplifier into its linear region.

7.2.Exact negative-feedback equation

Let a fraction $H\,V_{out}$ of the output be returned to the inverting side of a subtractor.
The resulting error and feedback paths are identified in Figure 83.

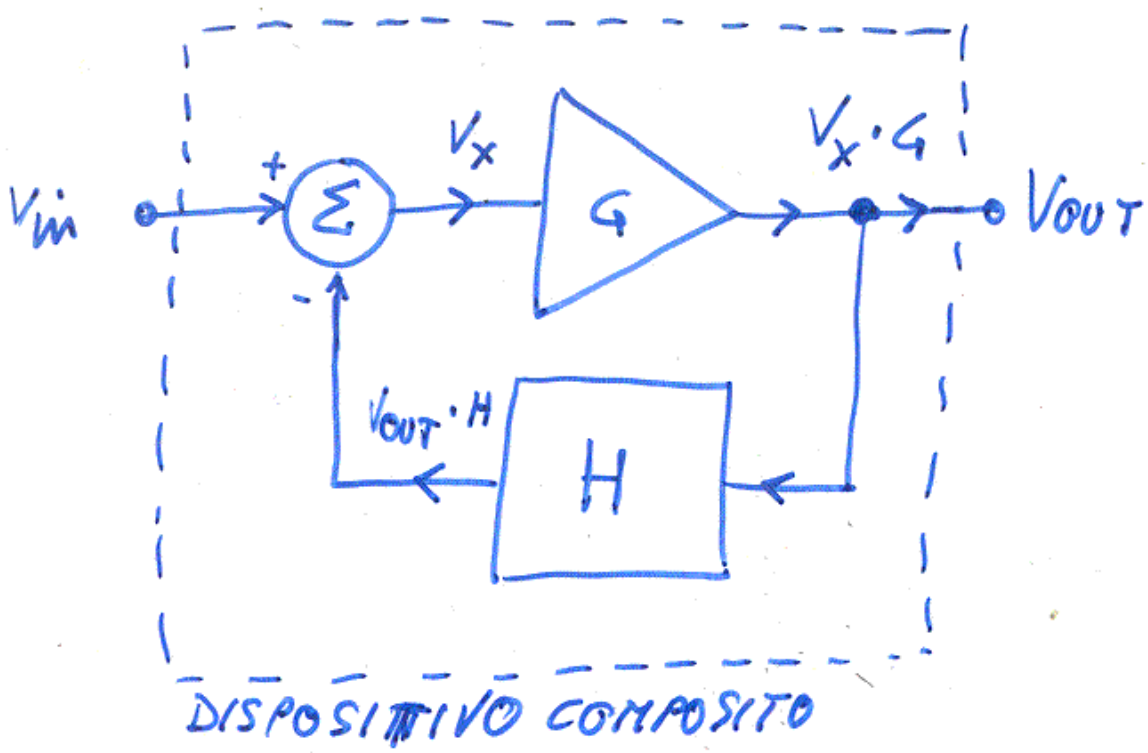


Figure 83. Closed-loop system with forward gain, feedback path and error-summing node.

The error signal is

$$V_x = V_{in} - H V_{out}\,. \tag{137}$$

The forward amplifier gives

$$V_{out} = G V_x = G(V_{in} - H V_{out})\,. \tag{138}$$

Collecting the output terms,

$$V_{out}(1 + GH) = G V_{in}, \tag{139}$$

and the exact closed-loop gain is

$$A_v = \frac{V_{out}}{V_{in}} = \frac{G}{1 + GH} = \frac{1}{1/G + H}\,. \tag{140}$$

When the loop gain $GH \gg 1$,

$$A_v \simeq \frac{1}{H}\,. \tag{141}$$

The passive feedback network can be made much more accurate and stable than the transistor-level open-loop gain, so the closed-loop gain becomes substantially independent of G. Its fractional sensitivity to a change in G is

$$\frac{dA_v/A_v}{dG/G} = \frac{1}{1 + GH}\,. \tag{142}$$

This result makes explicit the central engineering benefit of negative feedback: high loop gain suppresses forward-gain uncertainty. It also establishes the boundary of the approximation. At frequencies where G has fallen, or for a requested closed-loop gain approaching G, the gain is no longer determined solely by the feedback network.

7.3.Virtual equality of the input voltages

From the open-loop law,

$$V_+ - V_- = \frac{V_{out}}{A_{OL}}\,. \tag{143}$$

For a finite output and very large A_{OL},

$$V_+ \simeq V_-\,. \tag{144}$$

This is the virtual-short rule. It states equality of voltage, not a physical connection and not current flow between the terminals. It is valid only when all of the following conditions hold:

1. negative feedback is actually present;
2. the amplifier is operating linearly rather than saturated;
3. the input common-mode voltage is inside its permitted range;
4. the demanded output voltage and current are within the device limits;
5. the loop retains sufficient gain and stable phase at the frequency of interest.

The second ideal rule, $I_+ = I_- = 0$, follows from infinite input resistance. Together these rules permit the standard closed-loop derivations.

7.4.Non-inverting amplifier and voltage follower

In the non-inverting configuration, $V_+ = V_{in}$. A divider with R_1 from output to the inverting node and R_2 from that node to ground returns

$$H = \frac{R_2}{R_1 + R_2} \tag{145}$$

of the output. For large loop gain,

$$A_v \simeq \frac{1}{H} = \frac{R_1 + R_2}{R_2} = 1 + \frac{R_1}{R_2}. \tag{146}$$

The gain is positive and cannot be less than unity in this topology.

If the entire output is returned directly to the inverting input, $H = 1$ and

$$V_{out} \simeq V_{in}. \tag{147}$$

This is the voltage follower.

The unity-feedback connection and isolated load are shown in Figure 84.

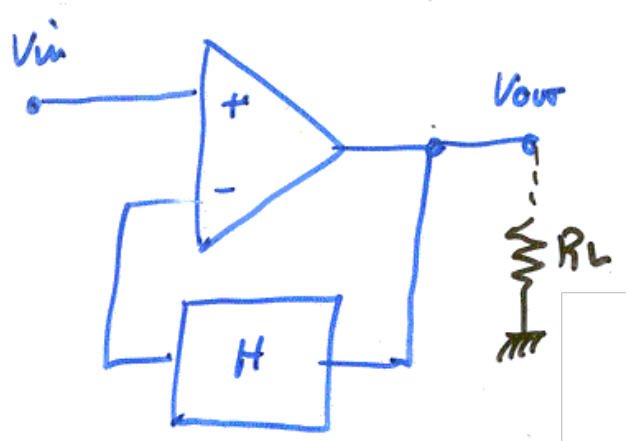


Figure 84. Feedback amplifier driving a load; unity feedback gives the voltage-follower case.

It offers a very high input resistance to the source and a low output resistance to the load. If a source resistance R_s directly drives a load R_L, the load voltage is

$$V_L = V_{in} \frac{R_L}{R_s + R_L}. \tag{148}$$

With an ideal follower between them, source current is negligible and the output drives R_L, so $V_L \simeq V_{in}$. The follower is therefore an impedance adapter or buffer, not a voltage-gain stage.

Two apparently different limiting cases produce $H = 1$. Setting the upper divider resistor to zero gives direct feedback. Letting the lower resistor tend to infinity removes the shunt to ground. A finite series resistor between output and the inverting input still has no voltage drop in the ideal model because the input current is zero; it therefore also produces unity feedback. A resistor from output to ground merely loads the output and is not part of the feedback ratio when direct feedback remains present.

7.5.Effects of finite input and output resistance

If the operational amplifier has finite input resistance R_{IN}, a source resistance R_3 attenuates the non-inverting input:

$$V'_{+} = V_{in}\frac{R_{IN}}{R_3 + R_{IN}}. \tag{149}$$

At the inverting input, R_{IN} loads the lower feedback resistor. The divider becomes

$$H' = \frac{R_2 \parallel R_{IN}}{R_1 + (R_2 \parallel R_{IN})}. \tag{150}$$

Thus finite input resistance can alter both the applied input and the nominal feedback gain. The external resistance scale must remain much smaller than the relevant input resistance.

With finite output resistance R_o, a load R_L attenuates the internal output:

$$V_o^{*} = V_o\frac{R_L}{R_o + R_L}. \tag{151}$$

The load factor $k' = R_L/(R_o + R_L) < 1$ can be regarded as a reduction of the forward gain to $G' = k'G$. Negative feedback still makes the closed-loop gain approximately $1/H$ if $G'H \gg 1$. This does not mean that output resistance and load current cease to matter. The demanded internal voltage rises, available output swing falls, dissipation increases, and the output-current limit is eventually reached.

7.6.Inverting amplifier

For the inverting amplifier, the non-inverting terminal is grounded. Negative feedback therefore holds the inverting summing node at approximately zero volts: a virtual ground. Let R_1 connect V_{in} to the summing node and R_2 connect the output to it. With zero input current into the amplifier, Kirchhoff's current law gives

$$\frac{V_{in} - 0}{R_1} + \frac{V_{out} - 0}{R_2} = 0. \tag{152}$$

Therefore

$$V_{out} = -V_{in}\frac{R_2}{R_1}, \quad A_v = -\frac{R_2}{R_1}. \tag{153}$$

The same result follows by superposition.

The resistor-defined inverting stage is shown in Figure 85.

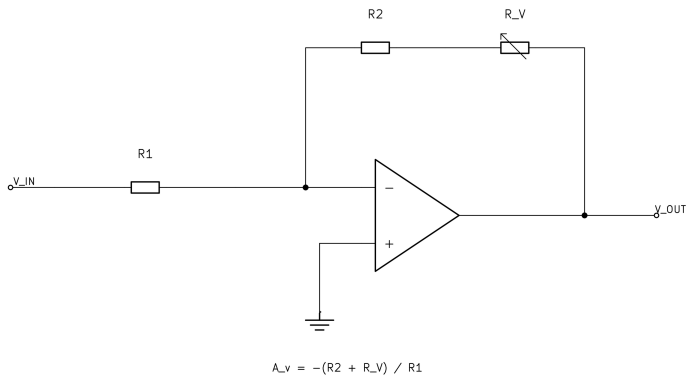


Figure 85. Inverting amplifier used for controlled gain or attenuation.

The contribution at the summing node from V_{in}, with V_{out} set to zero, is

$$V'_A = V_{in}\frac{R_2}{R_1 + R_2}\,. \tag{154}$$

The contribution from V_{out}, with V_{in} set to zero, is

$$V''_A = V_{out}\frac{R_1}{R_1 + R_2}\,. \tag{155}$$

The virtual-ground condition requires $V'_A + V''_A = 0$, which again gives $V_{out} = -V_{in}R_2/R_1$.

The gain magnitude is greater than one when $R_2 > R_1$, equal to one when $R_2 = R_1$, and less than one when $R_2 < R_1$. Unlike the non-inverting amplifier, the source sees a finite input resistance. Because the summing node is at virtual ground,

$$R_{in,stage} \simeq R_1\,. \tag{156}$$

This is an important distinction: the operational-amplifier input itself may draw negligible current, but the complete inverting circuit draws V_{in}/R_1 through its external input resistor.

A variable feedback resistance $R_2 + R_V$ produces

$$A_v = -\frac{R_2 + R_V}{R_1}, \tag{157}$$

so the gain varies without changing the stage input resistance. Placing the variable resistance in the input arm gives

$$A_v = -\frac{R_2}{R_1 + R_V}, \tag{158}$$

but changes input impedance together with gain. Feedback-side gain adjustment avoids that coupling. Taking an input resistance toward zero does not create infinite useful closed-loop gain: the result approaches the finite open-loop behaviour, violates the $GH \gg 1$ approximation, demands excessive source current, and is not a valid precision design.

7.7.Gain classes

Linear voltage stages can be classified by sign and magnitude:

- $A_v > 0$: non-inverting response;
- $A_v < 0$: inverting response;
- $|A_v| < 1$: attenuation;
- $|A_v| = 1$: follower or unity inverter;
- $|A_v| > 1$: amplification.

The sign and magnitude classes are summarised in Figure 86.

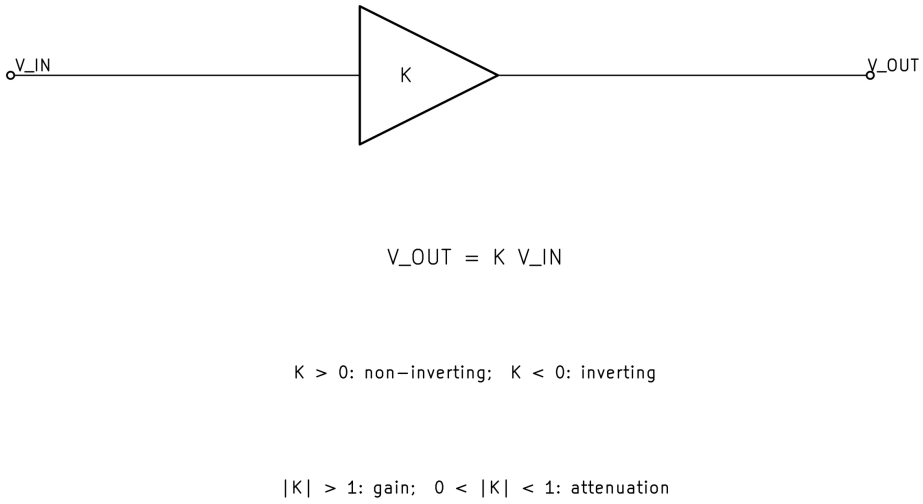


Figure 86. Sign and magnitude classification of a linear voltage stage.

This compact classification is useful throughout the conditioning chain because sign changes introduced by cascaded inverting stages must be included in the final transfer function, not treated as an afterthought.

7.8.Difference amplifier

The standard one-op-amp difference amplifier uses R_1 from V_2 to the inverting input, feedback resistor R_2, R_3 from V_1 to the non-inverting input, and R_4 from the non-inverting input to ground.

The four-resistor topology is shown in Figure 87. In Figures 87 and 88, $V_A=V_2$ and $V_B=V_1$.

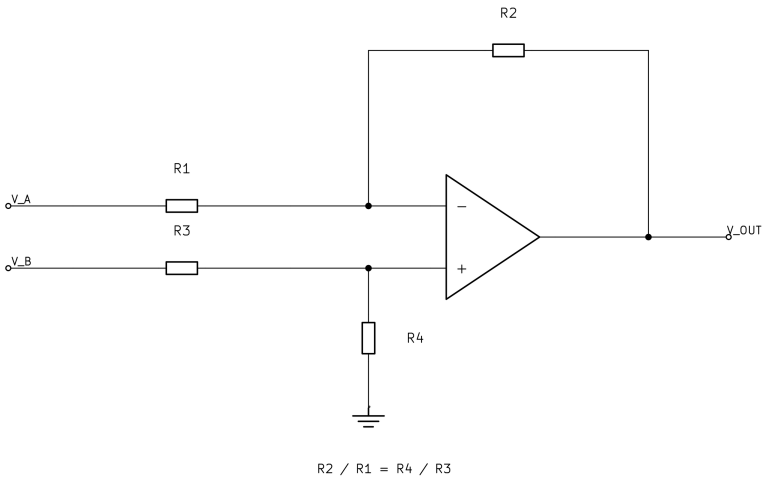


Figure 87. Four-resistor difference amplifier.

The non-inverting input voltage is

$$V_+ = V_1 \frac{R_4}{R_3 + R_4}\,. \tag{159}$$

To derive the full output, first apply the non-inverting gain to this node and then add the inverting contribution of V_2:

$$V_{out} = V_1 \frac{R_4}{R_3 + R_4}\left(1 + \frac{R_2}{R_1}\right) - V_2 \frac{R_2}{R_1}\,. \tag{160}$$

Pure differential behaviour requires the two resistor ratios to match:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3} = \alpha\,. \tag{161}$$

Then

$$\frac{R_4}{R_3 + R_4} = \frac{\alpha}{1 + \alpha}, \tag{162}$$

and hence

$$V_{out} = \alpha(V_1 - V_2)\,. \tag{163}$$

With all four resistors equal, $V_{out} = V_1 - V_2$. The circuit amplifies, reproduces, or attenuates the difference according to whether α is greater than, equal to, or less than one.

The matching condition is fundamental. Nominally high op-amp CMRR does not guarantee high circuit CMRR if the four external resistor ratios are unequal. Common-mode voltage is then converted into a differential output error. The topology also loads the two sources unequally: the non-inverting path sees approximately $R_3 + R_4$, while the inverting path commonly presents an impedance on the order of R_1. This is undesirable for high-impedance or mismatched transducers.

Adding a voltage follower to each source eliminates this loading. The buffers draw ideally zero sensor current and supply the resistor-network currents themselves. The subsequent difference stage retains

$$V_{out} = \frac{R_f}{R_i}(V_1 - V_2) \tag{164}$$

for matched resistor pairs, while the sensor-side input resistance becomes very high.

7.9.Referenced subtraction and summation

The non-inverting lower leg of a difference amplifier need not be tied to ground. If it is connected to a reference V_x, the output contains both the input difference and a controlled additive term. In the unity-ratio case,

$$V_{out} = V_1 + V_x - V_2\,. \tag{165}$$

Equivalently, a referenced unity difference stage can be written

$$V_{out} = (V_1 - V_2) + V_{ref}\,. \tag{166}$$

This is the basis for translating a bipolar sensor signal into a unipolar ADC range or placing a zero-input output at a desired bias voltage.

Insertion of the controlled reference is shown in Figure 88.

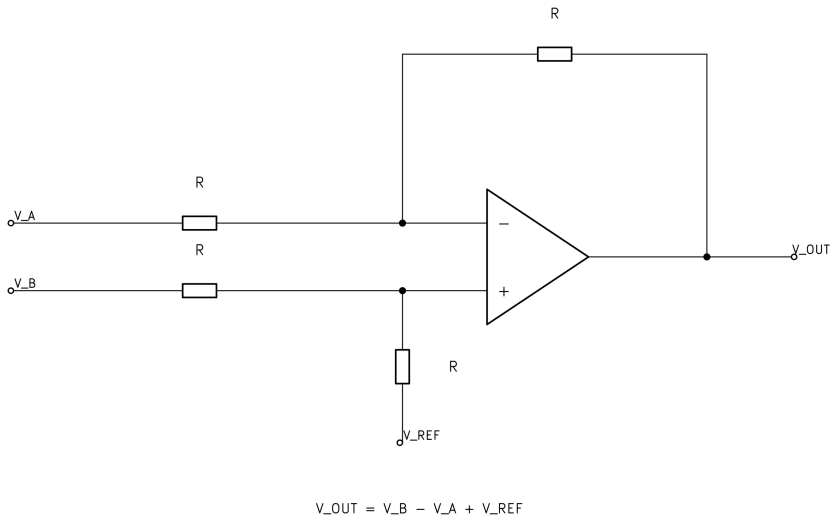


Figure 88. Difference stage with an added reference term for output-level translation.

A buffered reference divider is shown in Figure 89.

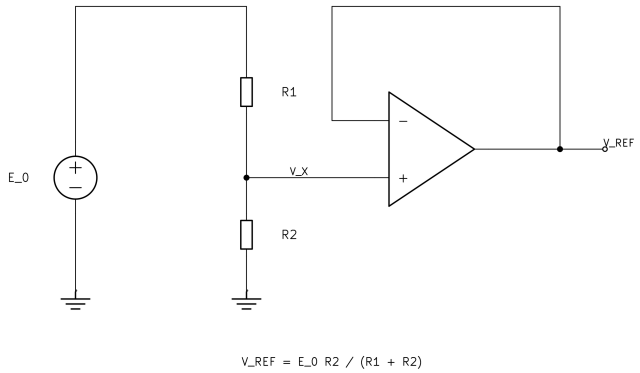


Figure 89. Buffered divider used to generate a reference voltage.

The inverting summing amplifier provides a more general linear combination. With input voltages $V_1, V_2, \ldots$ applied through $R_1, R_2, \ldots$ and feedback resistance R_f, summing-node KCL gives

$$V_{out} = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots\right). \tag{167}$$

For two inputs,

$$V_{out} = -V_1\frac{R_f}{R_1} - V_2\frac{R_f}{R_2}. \tag{168}$$

Independent variable series resistances $R_x = R_1 + R_{V1}$ and $R_y = R_2 + R_{V2}$ give independent weights

$$V_{out} = -V_1\frac{R_f}{R_x} - V_2\frac{R_f}{R_y}. \tag{169}$$

7.10.Representative parameter table and interpretation

The ideal model can be contrasted with representative real-device orders of magnitude:

Table 3. Representative parameter table and interpretation.

Parameter	Ideal model	Representative engineering range
Input resistance	infinite	10^5 to $10^9\ \Omega$
Output resistance	zero	1 to 100 Ω
Input current	zero	10^{-9} to 10^{-5} A
Maximum output current	unlimited	10^{-3} to 10^{-2} A
Linear input/output range	unlimited	often of order 10-15 V, supply dependent
Open-loop differential gain	infinite	10^4 to 10^6
Common-mode gain	zero	order unity before ratio interpretation
Input offset voltage	zero	millivolt order in the generic comparison table
Frequency dependence	none	open-loop gain falls with frequency
CMRR	infinite	approximately 80-100 dB in the generic table

These orders of magnitude illustrate the difference between the ideal operational-amplifier model and a real device.

7.11.Resistance-scale design rule

To avoid appreciable input loading, the surrounding resistances must be much less than the relevant amplifier input resistance. To avoid excessive output loading, the feedback/load resistance must be much greater than the output resistance. A useful ordering is

$$R_{OUT} \ll R_H \ll R_{IN}, \tag{170}$$

where R_H is a representative external network resistance. The suggested 10^3-$10^5\ \Omega$ range is a heuristic starting region, not a universal optimum.

Making every resistor very small reduces input-resistance error but forces the output to supply a large feedback current. For a non-inverting feedback divider,

$$I_H = \frac{V_{out}}{R_1 + R_2}. \tag{171}$$

This current consumes part of the output-current capability before the external load is driven. Conversely, very large resistances increase the voltage errors produced by the input currents.

7.12.Finite gain, bandwidth, and saturation

The exact feedback expression

$$A_v = \frac{A_{OL}}{1 + A_{OL}H} \tag{172}$$

must be used whenever $A_{OL}H$ is not much greater than one. Since real open-loop gain decreases with frequency, closed-loop gain accuracy also decreases at high frequency. The virtual-short approximation then develops a finite error

$$v_d = \frac{V_{out}}{A_{OL}(f)}. \tag{173}$$

The fall of open-loop gain with frequency limits the range over which the ideal closed-loop approximation remains accurate.

An amplifier also cannot produce arbitrary input or output voltages. A common-mode input range limits the permitted mean input voltage, even when the difference is small. Output swing is bounded by the supply rails and is usually load dependent. Once the amplifier saturates, $V_+ \simeq V_-$ is no longer a valid analysis rule.

7.13.Common-mode gain and resistor matching

With finite common-mode gain,

$$V_{out} = A_d v_d + A_{CM} v_{CM}. \tag{174}$$

A CMRR of 80 dB corresponds to an amplitude ratio of 10^4, and 100 dB corresponds to 10^5. The common-mode contribution, referred to the differential input, is approximately v_{CM}/CMRR. This device-level rejection is degraded by resistor-ratio mismatch in a discrete difference amplifier.

7.14.Input offset voltage and bias current

A real device can require a small differential input voltage V_{OS} to make its output zero. For a non-inverting or inverting amplifier using R_f and R_g, the first-order output contribution is approximately

$$V_{out,OS} \simeq \left(1 + \frac{R_f}{R_g}\right) V_{OS}. \tag{175}$$

This propagation equation makes the closed-loop consequence of input offset explicit.

Real input terminals also draw bias currents I_{B+} and I_{B-}. They create voltage drops in the source and feedback resistances. If the Thevenin resistance seen by the non-inverting input is R_+ and that seen by the inverting input is R_-, a first-order input-referred error is of the form

$$V_{IB} \simeq I_{B+}R_+ - I_{B-}R_-. \tag{176}$$

Equalizing the two resistance scales can cancel the part due to equal average bias current, but it cannot cancel unequal input currents or resistor mismatch.

7.15.Noise as an early-stage limitation

A real operational amplifier contributes an unwanted fluctuating component to the signal path. Its effect is most important before the first large gain because it is then amplified by every following stage.

8.Instrumentation amplifiers and precision front ends

High input impedance and a large nominal CMRR are useful only when the complete topology, resistor ratios, source impedances, internal nodes, and frequency response remain balanced and linear.

8.1.Why an instrumentation amplifier is required

Many measurement sources do not provide a useful voltage with respect to circuit ground. Instead, the quantity of interest is the small difference between two terminals that may both sit at a much larger voltage relative to the instrument. A physiological electrode pair is an obvious example, but the same problem occurs with bridge sensors, shunts, thermocouple arrangements, and remotely referenced transducers.

The front end must therefore perform three tasks simultaneously:

1.accept the two source terminals without materially loading them;

2.amplify their difference by an accurately known factor;

3.reject the voltage that is common to both terminals.

These requirements are stricter than the statement “amplify $v_P - v_N$.” The input impedances must be high and well balanced, the internal nodes must remain inside their common-mode and output-swing limits, and filtering or protection connected ahead of the amplifier must preserve symmetry.

8.2.Balanced and unbalanced source models

An ideal balanced source can be written as

$$v_P = v_{cm} + \frac{v_d}{2}, \quad v_N = v_{cm} - \frac{v_d}{2}. \tag{177}$$

If its physical midpoint is intentionally connected to the measurement reference, then v_{cm} is controlled.

The ideal balanced-source case is shown in Figure 90.

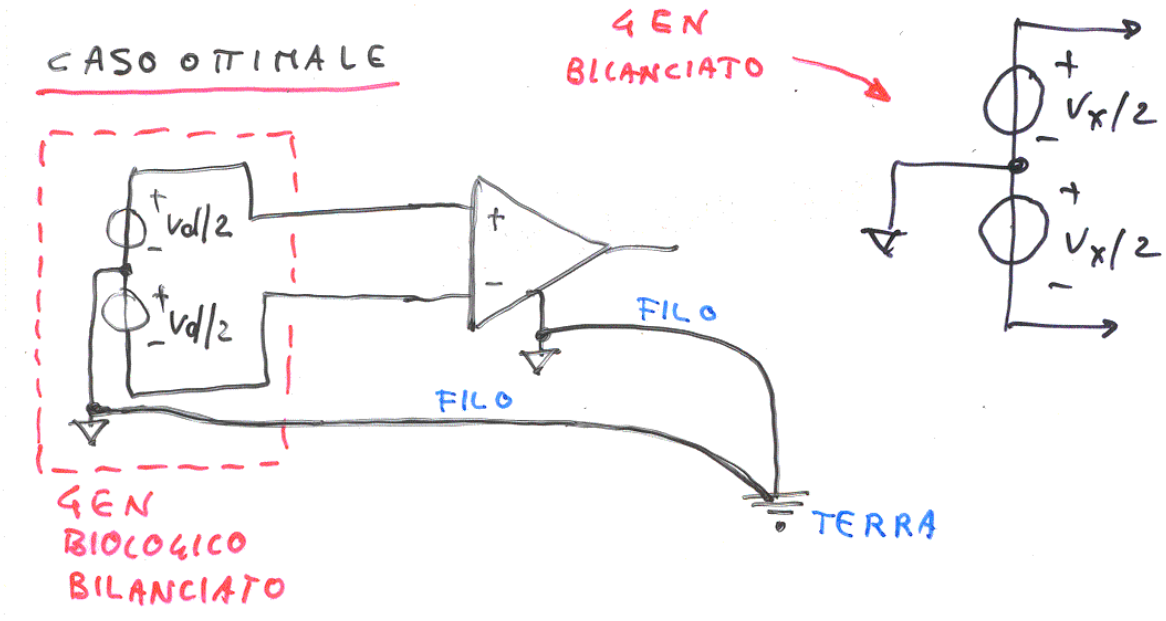


Figure 90. Balanced source with its electrical midpoint tied to the measurement reference.

A biological source is not automatically balanced in this ideal sense. Its two electrode impedances can differ, the body may float relative to the electronics, and capacitive coupling to the mains environment can move both electrodes together.

When the source has no reliable midpoint, an artificial centering network can be derived from the buffered first-stage outputs. Equal high-value resistors sample the low-impedance nodes v_A and v_B into a common node v_X without loading the electrodes directly. With no additional shunt load, superposition gives $v_X = (v_A + v_B)/2$, so the node tracks the first-stage common-mode voltage. A resistor R_Y may connect v_X to the chosen reference. For two equal sampling resistors R^*, the exact loaded result is

$$v_X = \frac{v_A + v_B}{2 + R^*/R_Y}, \tag{178}$$

which approaches the arithmetic mean when $R_Y \gg R^*$. The equal sampling arms are essential: unequal arms weight the two signal paths differently and contaminate the derived reference with differential signal.

The sampled reference node has a finite Thevenin impedance and should not directly drive circuitry that expects a stiff reference. A unity-gain buffer between the divider and the balancing-reference node preserves the sampled voltage while lowering its output impedance. In a single-supply system the final reference may also be translated around a mid-supply operating point; in a dual-supply system it may be centered around zero volts. This balancing reference remains an internal signal-processing node.

The equal-arm network and buffered centre reference are shown in Figure 91.

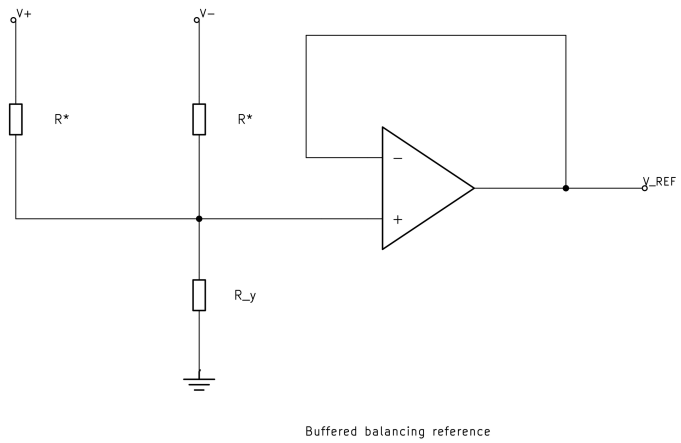


Figure 91. Artificial centre reference produced by an impedance-balanced divider and buffer.

8.3.The classical three-op-amp topology

The canonical instrumentation amplifier consists of two stages:

- a differential-input, differential-output stage made from two non-inverting operational amplifiers; and
- a differential-input, single-ended-output difference amplifier.

The first stage provides very high input impedance and most of the useful gain. The second stage subtracts the two first-stage outputs and establishes the relationship between the floating differential signal and the instrument's output reference.

The complete topology is shown in Figure 92 before its two stages are derived. In the drawing, $R_x=R_G$, $R_f' = R_f'' = R_F$, $V_{IN-}=v_N$ and $V_{IN+}=v_P$.

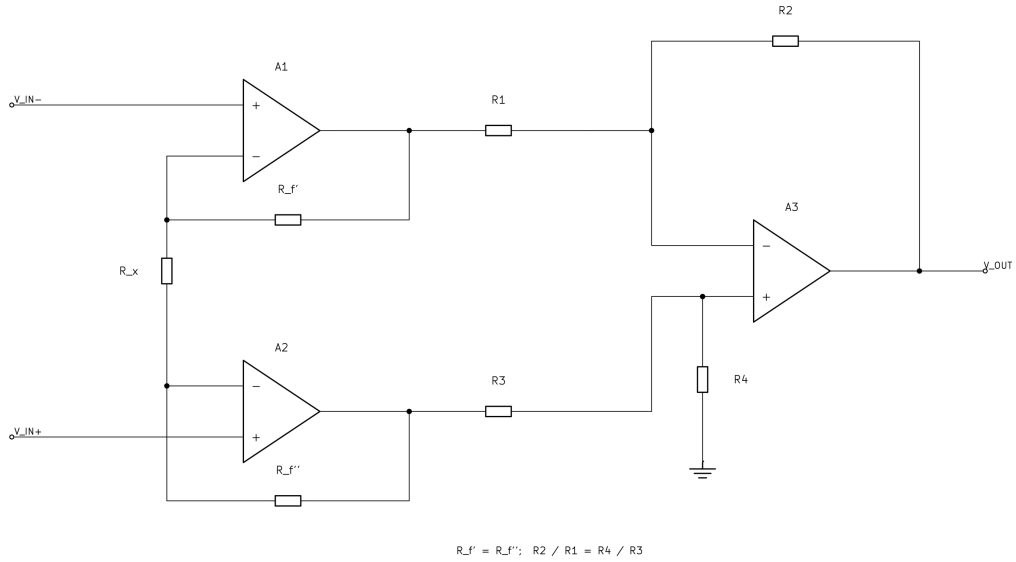


Figure 92. Three-operational-amplifier instrumentation topology with two input buffers and a matched difference stage.

8.3.1.First-stage derivation

Assume ideal operational amplifiers: infinite open-loop gain, infinite input resistance, zero input current, zero offset, and negative feedback that keeps each inverting input equal to its non-inverting input. Let the two feedback resistors both equal R_F, and let R_G join the inverting nodes.

Because the inverting nodes are at v_N and v_P, respectively, the current through R_G is

$$i_G = \frac{v_P - v_N}{R_G} = \frac{v_d}{R_G}. \tag{179}$$

No current enters either op-amp input, so this same differential current must flow through the two feedback resistors. The output voltages are therefore

$$v_A = v_N - \frac{R_F}{R_G} v_d, \tag{180}$$

$$v_B = v_P + \frac{R_F}{R_G} v_d. \tag{181}$$

Substituting $v_P = v_{cm} + v_d/2$ and $v_N = v_{cm} - v_d/2$ gives the especially useful internal-node form

$$v_A = v_{cm} - \frac{G_1}{2} v_d, \quad v_B = v_{cm} + \frac{G_1}{2} v_d, \tag{182}$$

with

$$G_1 = 1 + \frac{2R_F}{R_G}. \tag{183}$$

Thus the differential output of the first stage is

$$v_B - v_A = G_1 v_d. \tag{184}$$

If the two feedback resistors are not identical and are denoted R_{F1} and R_{F2}, the ideal differential gain becomes

$$G_1 = 1 + \frac{R_{F1} + R_{F2}}{R_G}. \tag{185}$$

The unequal pair also shifts the average of v_A and v_B by a signal-dependent amount. An ideal following subtractor would remove that shift, but a real subtractor with finite common-mode rejection converts some of it into error. This is the practical reason for keeping the two first-stage feedback resistors closely matched even though the ideal differential-gain expression contains only their sum.

The important architectural result is that gain can be changed through one component, R_G, while the two signal paths remain nominally symmetrical. Decreasing R_G increases gain. In an integrated instrumentation amplifier, the feedback resistors and the critical subtractor network can be fabricated and laser-trimmed together, while R_G is either external or selected through factory-trimmed internal taps.

8.3.2.Output difference amplifier

Let the upper signal v_A feed the inverting input through R_3, with feedback R_4. Let the lower signal v_B feed the non-inverting input through R_5, with R_6 from that input to the output reference. In Figure 92, these four resistors are labelled $\mathrm{R}_1, \mathrm{R}_2, \mathrm{R}_3$ and R_4, respectively. For an ideal op amp and zero reference voltage,

$$v_o = \left(1 + \frac{R_4}{R_3}\right)\frac{R_6}{R_5 + R_6}v_B - \frac{R_4}{R_3}v_A\,. \tag{186}$$

Define the two resistor ratios

$$k_1 = \frac{R_4}{R_3}, \quad k_2 = \frac{R_6}{R_5}\,. \tag{187}$$

When the ratios are equal, $k_1 = k_2 = k$, the expression reduces to

$$v_o = k(v_B - v_A), \tag{188}$$

so that

$$G_2 = k, \quad G_D = \left(1 + \frac{2R_F}{R_G}\right)k\,. \tag{189}$$

The most common implementation uses $k = 1$, often by choosing all four subtractor resistors equal. The second stage then performs a unity-gain subtraction and the complete gain is controlled by R_G alone.

8.3.3.Why ratio matching, rather than absolute value, controls CMRR

The subtractor rejects common mode only if its two transfer coefficients match. With arbitrary k_1 and k_2, the coefficient multiplying a common voltage applied to both v_A and v_B is

$$A_{cm} = \frac{k_2 - k_1}{1 + k_2}\,. \tag{190}$$

For the symmetrical differential component, the gain is

$$A_d = \frac{k_1 + k_2 + 2k_1k_2}{2(1 + k_2)}\,. \tag{191}$$

The common-mode rejection ratio is consequently

$$\mathrm{CMRR} = \left|\frac{A_d}{A_{cm}}\right|, \quad \mathrm{CMRR}_{dB} = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right|\,. \tag{192}$$

For a unity-gain subtractor with a small fractional ratio mismatch ϵ, the second-stage result is approximately

$$\mathrm{CMRR}_2 \simeq \frac{2}{|\epsilon|}\,. \tag{193}$$

If the first stage has ideal common-mode transfer and differential gain G_1, that stage multiplies the wanted differential component before the subtractor. The instrumentation-amplifier rejection limited by this subtractor mismatch is therefore approximately

$$\mathrm{CMRR}_{IA,\mathrm{mismatch}} \simeq G_1\mathrm{CMRR}_2 \simeq \frac{2G_1}{|\epsilon|}, \tag{194}$$

before finite operational-amplifier CMRR and frequency-dependent mismatches are included.

This makes the design sensitivity clear. Four individually accurate resistors do not automatically form two accurately equal ratios. Temperature coefficients must track as well as initial values. Integrated resistor networks generally outperform unrelated discrete resistors because their ratios and thermal histories are controlled together.

A second-stage ratio trim can be adjusted while equal voltages are applied to both inputs. Minimizing the output minimizes A_{cm}. This can correct a static ratio error at the trim frequency, but it does not guarantee high rejection over temperature or frequency. Input RC mismatch, op-amp input capacitance, parasitic capacitance, and finite device CMRR can make the optimum adjustment frequency-dependent.

8.4.Ideal assumptions and the real input model

The ideal derivation assumes:

- exact resistor values and exact resistor ratios;
- perfectly differential behaviour in both stages;
- infinite amplifier input resistance;
- zero input bias current;
- infinite open-loop gain;
- zero input offset voltage;
- no noise, no bandwidth limit, and no output limit.

A useful first-order real input model consists of a large but finite resistance in parallel with an input-current source, plus a small series voltage source representing input offset. This model explains three distinct errors.

First, finite input resistance loads the source. If a source voltage v_s with Thevenin resistance R_S drives an input resistance R_{in}, the amplifier input voltage v_{in} is given by

$$\frac{v_{in}}{v_s} = \frac{R_{in}}{R_S + R_{in}}\,. \tag{195}$$

With two inputs, unequal loading is more damaging than equal loading because it directly creates a differential error from common mode.

Second, bias current flowing through source resistance creates a voltage. With source resistances R_{S+} and R_{S-},

$$e_{IB} \simeq I_{B+}R_{S+} - I_{B-}R_{S-}\,. \tag{196}$$

Writing $I_{B\pm} = I_B \pm \Delta I_B/2$ and $R_{S\pm} = R_S \pm \Delta R_S/2$ shows the two useful first-order terms:

$$e_{IB} \simeq I_B\Delta R_S + \Delta I_B R_S\,. \tag{197}$$

Matching the source impedances cancels the effect of the average bias current; selecting an amplifier with low input-offset current controls the remaining term.

Third, input offset voltage behaves like a small unwanted differential source. Even when the external input is zero, the output is approximately $G_D V_{OS}$ until limited by the output range. Offset also drifts with temperature and time, so a one-time null does not remove the need for a low-offset, low-drift input stage.

8.5.Differential, common-mode, and output operating limits

An ideal amplifier accepts any v_d and v_{cm}. A real amplifier has several simultaneous limits:

1. **Absolute input voltage.** Neither input pin may exceed the device's absolute ratings, even if the differential voltage is small.
2. **Input common-mode range.** The internal input stage operates correctly only over a specified interval relative to the supply rails.
3. **Maximum differential input.** Protection structures and input transistors impose a limit on $|v_P - v_N|$.
4. **First-stage output swing.** In the three-op-amp topology the internal outputs are $v_{cm} \pm G_1 v_d/2$; they can saturate before the final output does.
5. **Difference-stage input range.** Both v_A and v_B must remain valid inputs for the second stage.
6. **Final output swing and output current.** The required v_o must fit inside the load-dependent output range.

The simultaneous differential and common-mode input components are shown in Figure 93. Here $V_{IN}=v_d$ and $V_C=v_{cm}$.

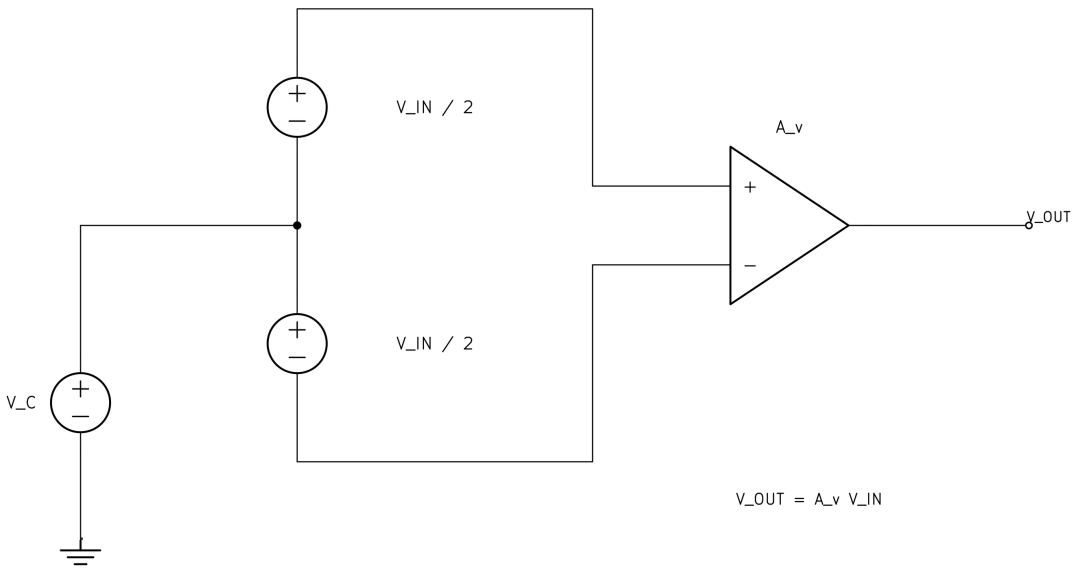


Figure 93. Differential input superimposed on a common-mode voltage.

For a symmetric first stage, a compact headroom test is

$$V_{OA,min} < v_{cm} - \frac{G_1 v_d}{2} < V_{OA,max}, \tag{198}$$

$$V_{OB,min} < v_{cm} + \frac{G_1 v_d}{2} < V_{OB,max}\,. \tag{199}$$

These inequalities form a diamond-shaped admissible region in the v_{cm}-v_d plane. Raising G_1 improves noise performance but narrows the differential range available at a given common-mode voltage. The final output must additionally satisfy

$$V_{o,min} < V_{REF} + G_D v_d < V_{o,max}\,. \tag{200}$$

This is why a data-sheet claim of high CMRR does not by itself establish that the circuit will work: CMRR is meaningful only while every internal and external node remains in its linear region.

Signal rejection must be distinguished from survival. A common-mode input outside the accepted range may produce an incorrect output, delayed recovery, or physical damage. Input filtering and common-mode rejection do not replace protection against excessive voltage.

8.6.Electrode offset and the allocation of gain

Electrode interfaces can contribute a DC potential E_{el} much larger than the wanted AC signal. If a single stage applies gain G to both,

$$v_o = G[v_s(t) + E_{el}], \tag{201}$$

and the no-clipping condition is

$$G \le \frac{V_{o,pk,max}}{\max|\,v_s(t) + E_{el}\,|}\,. \tag{202}$$

The numerical example uses approximately $v_{s,pk} = 5\ \mathrm{mV}$, $E_{el} = 100\ \mathrm{mV}$, and $V_{o,pk,max} = 9\ \mathrm{V}$. Ignoring offset would suggest a gain near 1800; including it limits the admissible gain to $9/0.105 = 85.7$. A practical selection must remain at or below that value—typically 80 to 85 before any additional margin is reserved. A modest DC error can therefore consume almost all the headroom intended for a millivolt signal.

The proposed architecture is therefore:

1. use the highest first-stage gain that remains linear for the worst credible electrode offset and common-mode voltage;
2. remove the unwanted DC component with a high-pass coupling network; and
3. apply the remaining AC gain in a later stage.

For a simple coupling capacitor C and bias resistor R,

$$f_L = \frac{1}{2\pi RC}\,. \tag{203}$$

An application-dependent lower corner on the order of 0.1 to $1\ \mathrm{Hz}$ may be chosen well below the lowest useful signal frequency. The total AC gain in band is $G_1 G_2$, but only G_1 acts on the large DC electrode offset. The recovery time after connection or a large transient is set by the high-pass time constant and must be included in the implementation requirements.

8.7.Noise and the first-stage imperative

Noise introduced before the first gain stage is amplified by every later stage. Noise introduced later has less effect when referred to the input because it is preceded by gain. The first stage should therefore provide the largest gain compatible with the available offset and common-mode headroom.

The effect of introducing noise before and after the first gain is shown in Figure 94.

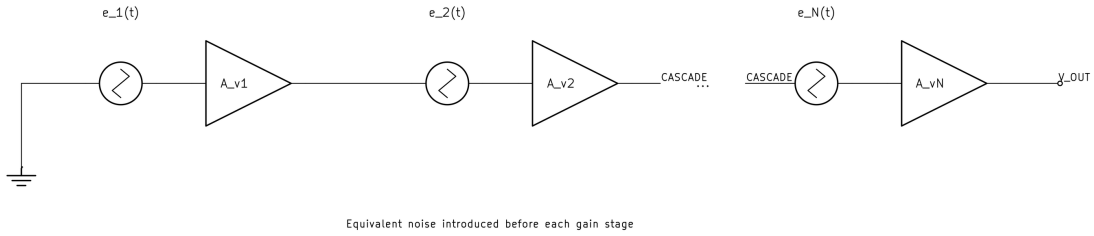


Figure 94. Cascaded gain stages with noise contributions introduced at successive nodes.

9.Gain selection, offset adjustment, error propagation, and calibration

The gain and offset controls establish the affine map between the transducer signal and the required output range. Residual non-correspondence, hysteresis, noise, self-heating, and bandwidth limitations must still be treated separately because they are not removed by zero and span adjustment.

9.1.Gain strategy and robust switching

Continuously variable gain is unnecessary when a small set of defined ranges is sufficient. A sequence such as 1, 2, 5, 10, 20, 50, 100, 200, 500 provides predictable scaling and works naturally with oscilloscopes, converters, and recorders. In an instrumentation amplifier the preferred range-setting element is R_G because changing one resistor adjusts the first-stage differential gain while preserving the two input paths.

A sliding contact or ordinary trimmer directly in the high-gain R_G path is discouraged. Contact resistance may be unstable and can inject broadband disturbance into the entire chain. Integrated amplifiers with factory-trimmed gain taps, or fixed precision resistors selected by low-leakage switches, are more repeatable.

When gain is changed in a later op-amp stage, switch topology matters:

- A selector that momentarily opens the feedback path lets the amplifier operate at open-loop gain and usually drives it into saturation.

The unsafe open-feedback state is shown in Figure 95.

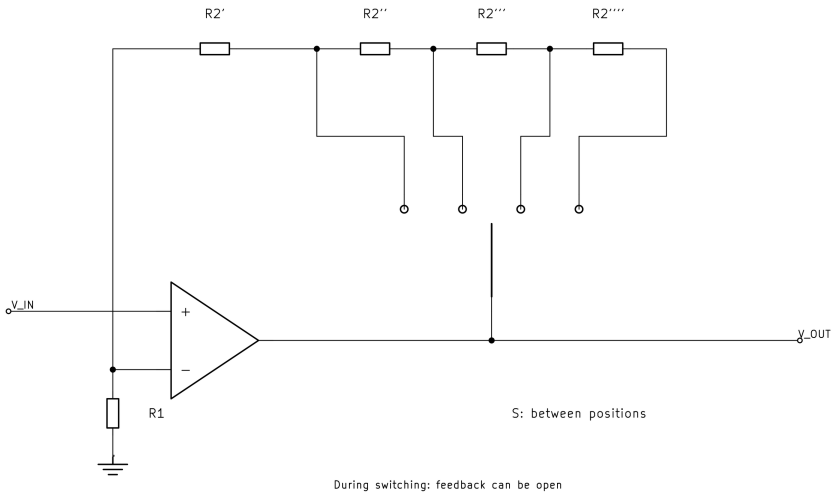


Figure 95. Selectable-gain arrangement that can leave an operational amplifier without feedback.

- In a non-inverting stage, switching the grounded feedback leg can make the transition tend toward unity gain rather than infinity.
- In an inverting stage, an always-connected fallback feedback resistor can guarantee a finite maximum gain if the selector opens.

The permanent feedback path that bounds gain is shown in Figure 96.

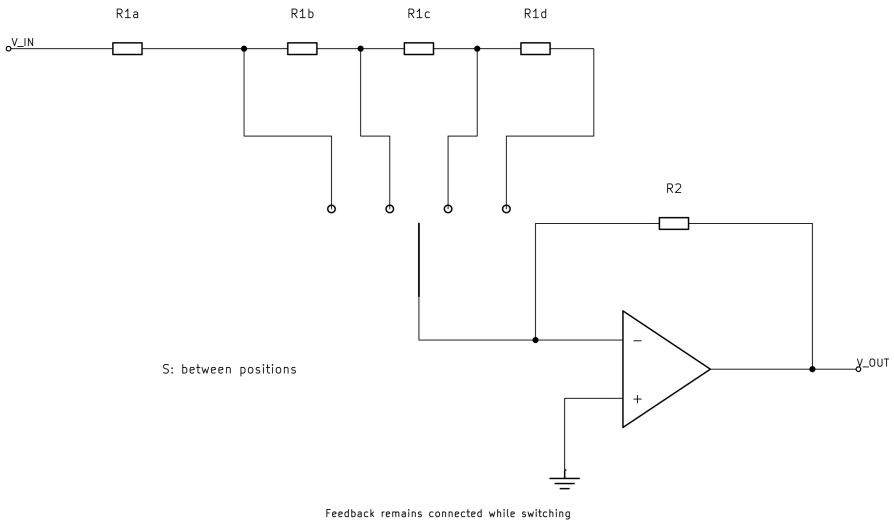


Figure 96. Bounded selectable-gain network with a permanent feedback contribution.

- A resistive attenuator ahead of a fixed-gain buffer keeps the active stage's feedback constant, but its Thevenin resistance varies with position and is loaded by finite input resistance unless buffered.

The attenuator-before-fixed-gain alternative is shown in Figure 97.

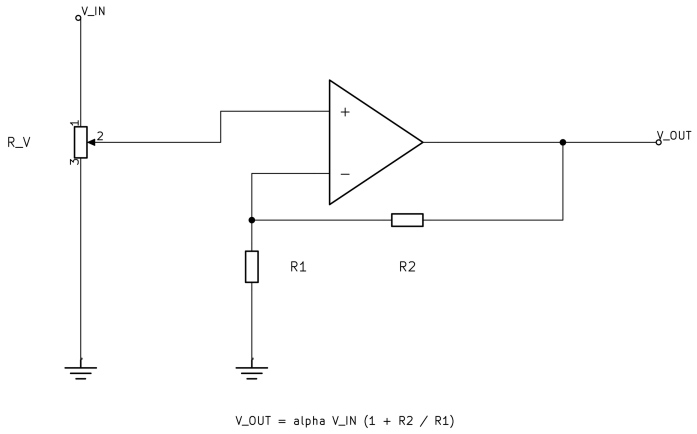


Figure 97. Variable attenuator followed by an amplifier with fixed feedback gain.

Every permitted selector position must leave a defined DC feedback path and a bounded output.

Noise considerations constrain gain distribution. Noise introduced at the first stage is amplified by every later stage, while noise introduced later is divided by the preceding gain when referred to the system input. The first stage should therefore combine low intrinsic noise with as much fixed gain as headroom permits. Wide gain variation is then assigned to later stages where its noise contribution is less influential.

9.2.Offset compensation and independent calibration

The conceptual offset correction is simple: if the amplifier chain produces an unwanted output offset V_{OFF}, sum an equal and opposite correction. The difficulty is that the actual offset is unknown within a range, drifts over time, and can have either sign. The adjustment circuit must cover the required range while adding little noise, drift, loading, or gain error.

A variable bipolar correction generator can be formed with a potentiometer connected between $+E_0$ and $-E_0$. With normalized wiper position $0 \leq \alpha \leq 1$, it produces

$$V_X = E_0(2\alpha - 1)\,. \tag{204}$$

Precision bipolar references may instead be produced from a stable positive reference and a unity-gain inverter. The inverter's two resistors should be equal, thermally matched, and paired with a low-offset, low-drift op amp so that $-E_0$ tracks $+E_0$.

The raw $\pm E_0$ range is usually much larger than the required correction. An inverting summing stage attenuates it by a resistor ratio. If the offset input resistor is R_X and the feedback resistor is R_Y,

$$|V_{OFF,max}| = E_0 \frac{R_Y}{R_X}\,. \tag{205}$$

Selecting $R_X \gg R_Y$ narrows the trim range. The load placed by R_X on the potentiometer should also be small, which requires $R_X \gg R_P$, where R_P is the potentiometer resistance. Current drawn from the reference generator and delivered by its inverter must remain below their output-current limits.

The worked design uses a nominal $E_0 = 5\ \mathrm{V}$, a desired correction of $\pm 100\ \mathrm{mV}$, and a nominal $R_Y = 10\ \mathrm{k\Omega}$. The required ratio is

$$\frac{R_Y}{R_X} = \frac{0.1}{5} = \frac{1}{50}, \tag{206}$$

so $R_X = 500\ \mathrm{k\Omega}$. A $20\ \mathrm{k\Omega}$ potentiometer is then much smaller than R_X, so loading-induced nonlinearity is limited.

Gain trim and offset trim must be orthogonal.

The separation of coefficient and translation controls is summarised in Figure 98.

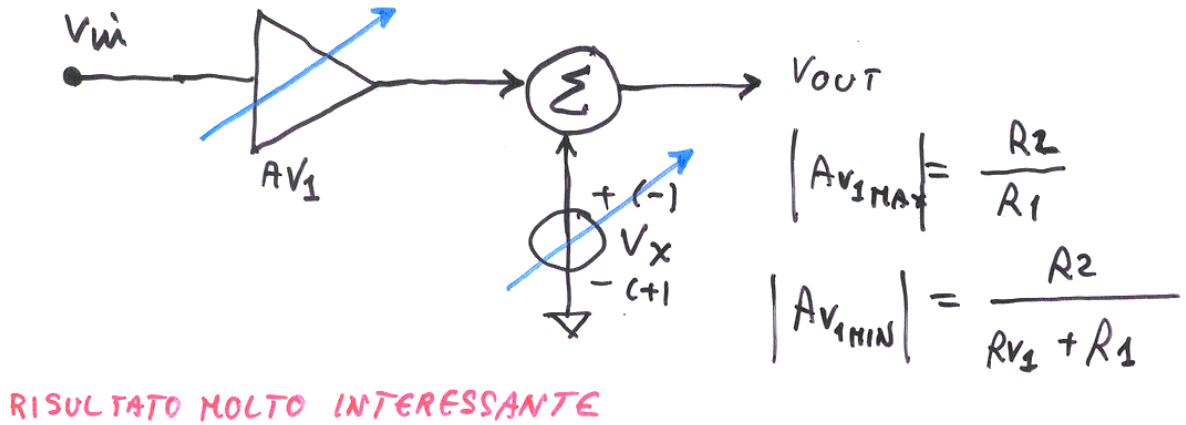


Figure 98. Block representation of independent gain and offset control.

A weighted inverting summer assigns the signal and correction to separate summing resistors:

$$v_o = -v_i \frac{R_2}{R_1 + R_{V1}} - V_X \frac{R_2}{R_3}\,. \tag{207}$$

Changing R_{V1} adjusts the signal coefficient, while changing V_X adjusts the offset term. The implemented circuit must preserve these separate summing paths and use the stated non-inverting reference connection.

The corresponding separate signal and reference paths are shown in Figure 99.

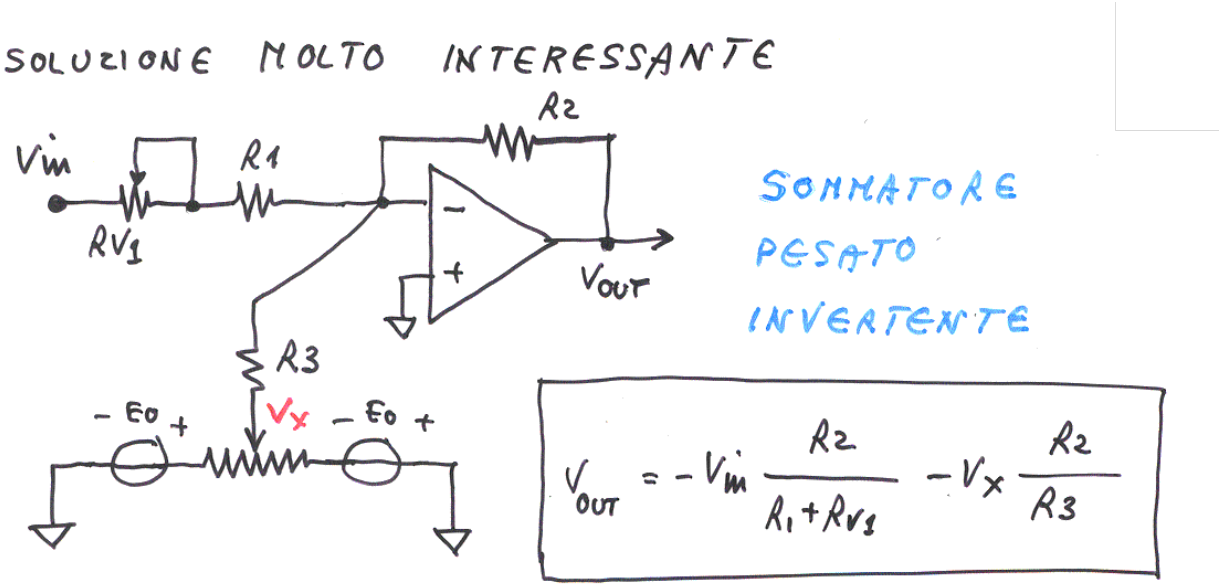


Figure 99. Independent signal-gain and reference-translation paths in a conditioning stage.

9.3.Intermediate gain, translation, and fine adjustment

Additional gain can be placed after the filter bank because a single large front-end gain may exceed internal headroom, while filtering before all amplification may leave the filter's own noise too prominent. The total gain can exceed 2000 when several stages are cascaded, but each stage remains in a moderate range.

9.3.1.Inverting switched-gain stage

The inverting implementation uses matched equal resistors and switches additional input paths to obtain integer gain magnitudes $|G| = 1, 2, 3, 4, 5$. With n equal active input conductances and feedback resistance R, the ideal signal gain is

$$G = -n\,. \tag{208}$$

An offset voltage can be summed through another resistor, and a capacitor in parallel with the feedback resistor introduces a pole even when the low-frequency gain is unity. Because gain depends mainly on resistor ratios, a common resistor network can provide better thermal tracking than unrelated absolute-value resistors.

Geometrically spaced gains such as $1, 2, 4, 8$ provide predictable range selection. Doubling analogue gain makes an otherwise under-filled converter use twice as many codes. It does not recover information already lost through sensor noise, amplifier noise, distortion, incomplete settling, or clipping.

9.3.2.Non-inverting resistor ladder

Alternative non-inverting networks use equal resistors arranged so that

$$G = 1 + \frac{R_F}{R_G}\,. \tag{209}$$

Representative gains of 2 and 5 can be obtained with equal elements that favor ratio tracking. This configuration preserves signal polarity but does not integrate an offset summing input as naturally as the inverting form.

9.3.3.Final independent gain and offset trim

The fine-adjustment stage is an inverting weighted summer. In the simplified model,

$$v_o = -v_{in}\frac{R}{R_2 + R_{V2}} - V_{off}\frac{R}{R_1}. \tag{210}$$

R_{V2} trims gain, while R_{V1} is the potentiometer that generates V_{off} between the positive and negative reference rails. Its wiper is coupled to the summing node through the fixed resistance R_1. Orthogonality and negligible loading of the offset potentiometer require

$$R_{V1} \ll R_1, \quad R_{V2} \ll R_2, \tag{211}$$

so each trimmer makes only a fine correction around a stable fixed-resistor value. This reduces adjustment interaction, contact sensitivity, and thermal drift. A feedback capacitor adds a final pole.

Hardware gain and zero trims are essential when the analogue output itself is the calibrated representation supplied to another instrument. If the signal is digitised locally, the same affine correction can often be applied numerically after a suitable uncalibrated analogue range has been guaranteed. Digital correction still cannot recover a clipped analogue signal.

9.4.Error model for the complete chain

The complete error model is organised by functional block.

9.4.1.Error classes

For a nominally linear transducer:

- zero or offset error shifts the entire characteristic;
- scale or sensitivity error changes its slope;
- nonlinearity changes slope as a function of input;
- self-heating and hysteresis can add further physical errors.

For the electronics:

- each amplifier can contribute gain error and input/output offset;
- the subtractor can have ratio error and zero error;
- the reference generator can have set-point error and drift;
- the excitation supply can have value error and drift;
- the filter can have DC gain error, offset, cutoff-frequency error, and phase variation;
- every active and passive block contributes noise and temperature dependence.

The dominant correctable effects are offset and gain. Noise and thermal drift form a third class that cannot be removed by a single static trim.

9.4.2.Excitation error becomes both zero and span error

Let the actual Pt100 current be $J + \delta J$. Then

$$v_T = (J + \delta J)(R_0 + \alpha T) \tag{212}$$

or

$$v_T = (J + \delta J)R_0 + (J + \delta J)\alpha T. \tag{213}$$

The first term is the intercept and the second is the temperature-dependent term. Excitation error changes both. Relative to the ideal model, a stable δJ can be represented as an equivalent transducer gain error with a corresponding baseline shift. This is why excitation belongs inside the calibrated measurement function, not outside it as an unrelated power-supply detail.

The simultaneous intercept and slope displacement is shown in Figure 100.

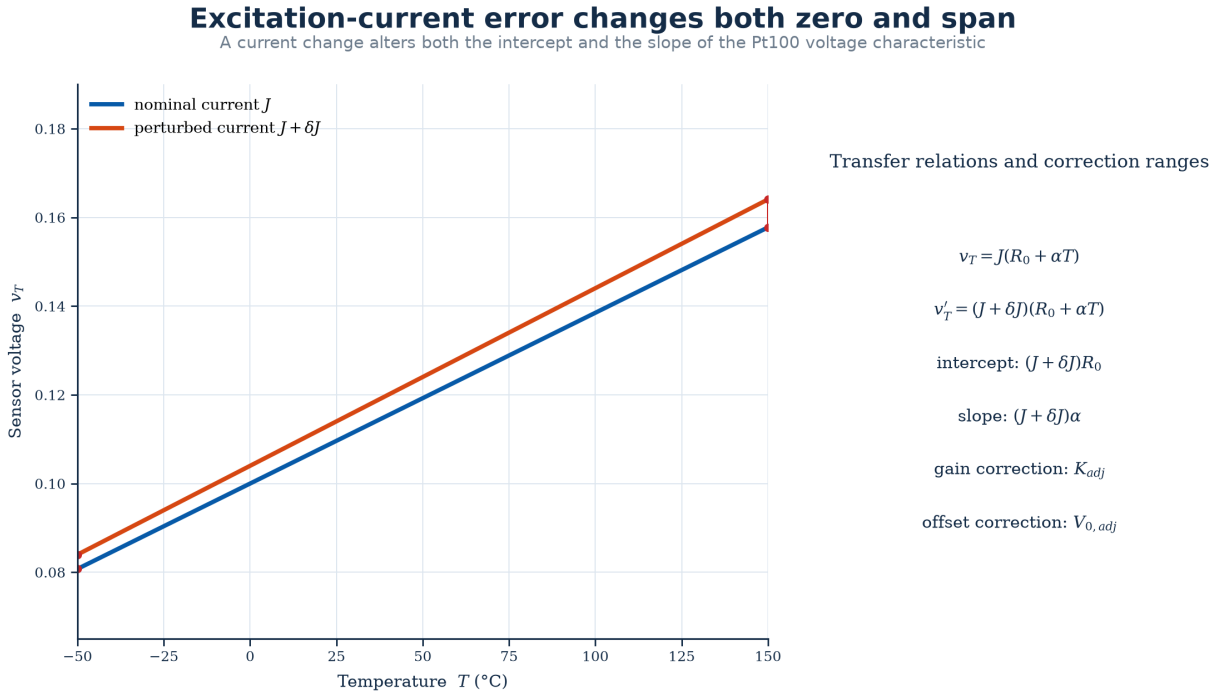


Figure 100. Nominal and perturbed Pt100 excitation characteristics with the required correction authority.

9.4.3.Referring distributed errors to the output

Represent stage i as

$$y_i = k_i y_{i-1} + b_i \,. \tag{214}$$

For n cascaded stages, the overall gain is

$$K = \prod_{i=1}^{n} k_i \,. \tag{215}$$

An offset introduced at stage i is multiplied by every downstream gain. The total output-referred offset is

$$E_{\text{out}} = b_n + k_n b_{n-1} + k_n k_{n-1} b_{n-2} + \cdots + \left(\prod_{j=2}^{n} k_j \right) b_1 \,. \tag{216}$$

Therefore the real chain can be reduced, for affine-error purposes, to

$$v_{real} = K_{eq} v_{ideal} + E_{eq}, \tag{217}$$

where K_{eq} is near one and E_{eq} is near zero after nominal design. Components with errors of opposite sign may appear to cancel, but random cancellation is not a reliable design method because tolerances and drifts change independently.

9.5.Two-point correction and calibration

Place an adjustment after the complete real chain:

The high-level ordering of conversion, excitation and final correction is shown in Figure 101. The drawing labels the corrected output $V_{OUT}^{*} = v_{corr}$.

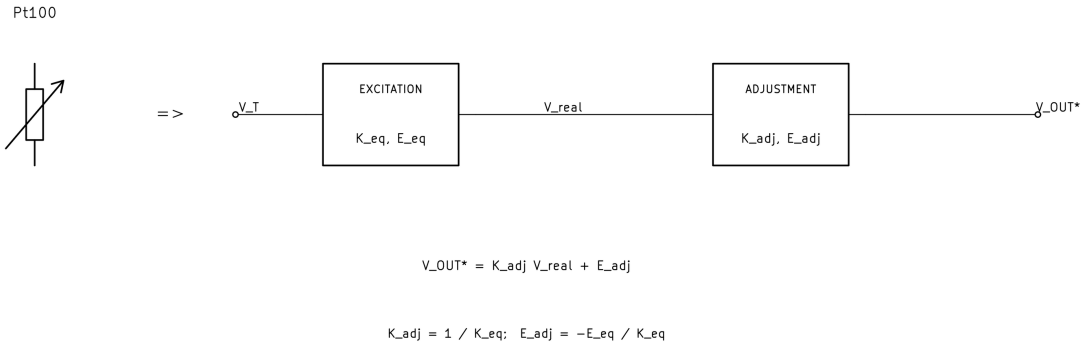


Figure 101. Pt100 conversion and excitation followed by a final adjustment stage.

$$v_{corr} = K_{adj} v_{real} + E_{adj}\,. \tag{218}$$

Exact affine correction requires

$$K_{adj} K_{eq} = 1, \tag{219}$$

and

$$K_{adj} E_{eq} + E_{adj} = 0\,. \tag{220}$$

Thus

$$K_{adj} = \frac{1}{K_{eq}}, \tag{221}$$

$$E_{adj} = -\frac{E_{eq}}{K_{eq}}\,. \tag{222}$$

The adjustment ranges must cover the full credible error bounds with margin:

$$\frac{1}{K_{eq,max}} \le K_{adj} \le \frac{1}{K_{eq,min}}, \tag{223}$$

with a corresponding bipolar range for E_{adj}.

A two-point calibration can use a precise reference transducer or an electrical substitute. For a Pt100 channel, precision resistors can reproduce two known temperatures: approximately $100\,\Omega$ for $0\,^{\circ}\mathrm{C}$ and $138.5\,\Omega$ for $100\,^{\circ}\mathrm{C}$ under the linear model.

Given two applied reference conditions whose ideal outputs are Y_L and Y_H, and whose measured uncorrected outputs are y_L and y_H,

$$K_{adj} = \frac{Y_H - Y_L}{y_H - y_L}, \tag{224}$$

$$E_{adj} = Y_L - K_{adj} y_L \,. \tag{225}$$

In a manual circuit, the practical sequence is to apply the lower reference and adjust zero, apply the upper reference and adjust gain, then repeat because the controls are not perfectly independent. Calibration removes stable affine error. It does not remove nonlinearity between the points, random noise, hysteresis, self-heating differences between calibration and use, or subsequent drift.

9.6.Worked design A: Pt100 over 0 to 100 °C

With $J = 1\,\mathrm{mA}$,

$$v_T(0) = 100\,\mathrm{mV}, \quad v_T(100) = 138.5\,\mathrm{mV}\,. \tag{226}$$

For a 0 to $10\,\mathrm{V}$ output,

$$G_T = \frac{10}{38.5\,\mathrm{mV}} = 259.74\,. \tag{227}$$

A one-stage affine form would require an output-referred translation

$$V_0 = -259.74(0.100) = -25.97\,\mathrm{V}, \tag{228}$$

which is outside the assumed electronics range. A feasible split with $E_0 = -5\,\mathrm{V}$ is

$$G_1 = \frac{5}{0.100} = 50, \tag{229}$$

so

$$v_x = 5.000\ldots6.925\,\mathrm{V}, \tag{230}$$

$$v_y = 0\ldots1.925\,\mathrm{V}, \tag{231}$$

and

$$G_2 = \frac{10}{1.925} = 5.195\,. \tag{232}$$

The electrically equivalent choice $J = 0.5\,\mathrm{mA}$ and $G_1 = 100$ produces the same internal voltages with one-quarter of the sensor dissipation:

$$v_x = G_1 J R(T) = 100(0.5\,\mathrm{mA})R(T)\,. \tag{233}$$

This example demonstrates the coupled choice of excitation current, first-stage gain, reference value, and second-stage gain.

9.7.Worked design B: Pt100 over -50 to +100 °C

Using the linear model and $J = 1\,\mathrm{mA}$,

$$R(-50) = 80.75\,\Omega, \quad R(100) = 138.5\,\Omega, \tag{234}$$

and

$$\Delta v_T = 57.75\,\mathrm{mV}\,. \tag{235}$$

If the desired output is -5 to $+10\,\mathrm{V}$, then

$$G_T = \frac{15}{57.75\,\mathrm{mV}} = 259.74\,. \tag{236}$$

Choosing $G_1 = 50$ and $E_0 = -5\,\mathrm{V}$ makes the $0\,^\circ\mathrm{C}$ condition the internal zero:

$$v_x(-50) = 4.0375\,\mathrm{V}, \tag{237}$$

$$v_x(0) = 5.0000\,\mathrm{V}, \tag{238}$$

$$v_x(100) = 6.9250\,\mathrm{V}\,. \tag{239}$$

After subtracting $5\,\mathrm{V}$, the internal range is -0.9625 to $+1.925\,\mathrm{V}$. With

$$G_2 \simeq 5.195, \tag{240}$$

the output becomes -5 to $+10\,\mathrm{V}$ and crosses zero at $0\,^\circ\mathrm{C}$.

For comparison, the alternative unipolar allocation is shown in Figure 102.

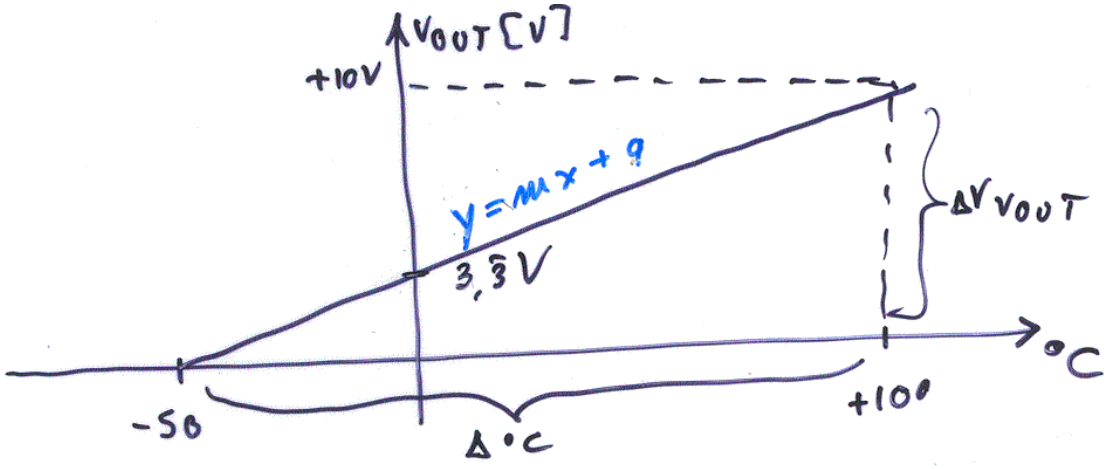


Figure 102. Alternative unipolar mapping of the Pt100 range from minus 50 to plus 100 degrees Celsius into a 0 to 10 volt output.

Expressing temperature in kelvin does not make a Pt100 characteristic pass through the origin. For $R = 100 + 0.385T_C$, the resistance does not vanish at $0\,\mathrm{K}$, so a translation remains unless the electrical variable is redefined as a compensated or extrapolated quantity. Changing the engineering-unit origin changes the conditioner, but a real Pt100 does not become origin-passing merely because the temperature axis is relabelled.

9.8.Worked design C: Pt100 over -50 to +150 °C with error allowance

A third worked example adds allowance for sensor and electronics error. The starting data are:

- Pt100 range: -50 to $+150\,^{\circ}\mathrm{C}$;
- linear model: $R = 100 + 0.385T\,\Omega$;
- excitation: $J = 1\,\mathrm{mA}$;
- four-wire differential input;
- desired A/D input: 0 to $10\,\mathrm{V}$;
- useful signal content extending from DC to approximately $5\,\mathrm{Hz}$;
- transducer and electronics tolerances to be corrected later.

The endpoint resistances and voltages are

$$R(-50) = 80.75\,\Omega, \tag{241}$$

$$R(150) = 157.75\,\Omega, \tag{242}$$

$$v_{T,min} = 80.75\,\mathrm{mV}, \quad v_{T,max} = 157.75\,\mathrm{mV}, \tag{243}$$

$$\Delta v_T = 77.00\,\mathrm{mV}\,. \tag{244}$$

The required nominal total gain is

$$G_T = \frac{10}{77\,\mathrm{mV}} = 129.87 \simeq 130\,. \tag{245}$$

If the first stage alone were allowed to reach $10\,\mathrm{V}$ at the upper endpoint,

$$G_{1,max} = \frac{10}{0.15775} = 63.39\,. \tag{246}$$

The exact internal translation required to zero the lower endpoint would then be

$$E_0 = -\,G_{1,max} v_{T,min} = -\,5.118\,\mathrm{V}, \tag{247}$$

which is close to, but not equal to, the convenient $-5\,\mathrm{V}$ reference. Selecting $E_0 = -\,5\,\mathrm{V}$ gives

$$G_1 = \frac{5}{0.08075} = 61.92, \tag{248}$$

$$G_2 = \frac{129.87}{61.92} = 2.097\,. \tag{249}$$

At the upper endpoint,

$$v_x = 61.92(0.15775) = 9.77\,\mathrm{V}, \tag{250}$$

so the first-stage output remains below the assumed $10\,\mathrm{V}$ limit. After translation, the second-stage input is approximately 0 to $4.77\,\mathrm{V}$, and the output is 0 to $10\,\mathrm{V}$.

The correction ranges follow from the error allocation. For an electronics gain error of approximately $\pm 2\%$, the reciprocal gain trim must cover about

$$K_{adj} \simeq 0.98 \ldots 1.02\,. \tag{251}$$

A wider practical range of approximately ± 5 to $\pm 6\%$ includes transducer scale error and adjustment margin.

For zero error, two illustrative worst-case terms are combined:

- a $\pm 2\%$ error on the $5\,\mathrm{V}$ reference gives $\pm 100\,\mathrm{mV}$ at the translation node; with $G_2 \simeq 2$, this is about $\pm 200\,\mathrm{mV}$ output-referred;
- a Pt100 zero error of $\pm 1\,\Omega$ gives $\pm 1\,\mathrm{mV}$ at $1\,\mathrm{mA}$; with total gain about 130, this is $\pm 130\,\mathrm{mV}$ output-referred.

Adding them worst-case gives an illustrative required offset-adjustment interval of approximately

$$-330\,\mathrm{mV} \leq E_{adj} \leq +330\,\mathrm{mV}\,. \tag{252}$$

For an implementation, the adjustment range must be calculated from the selected components and sensor specification.

The nominal endpoint map and separate adjustment ranges are collected in Figure 103.

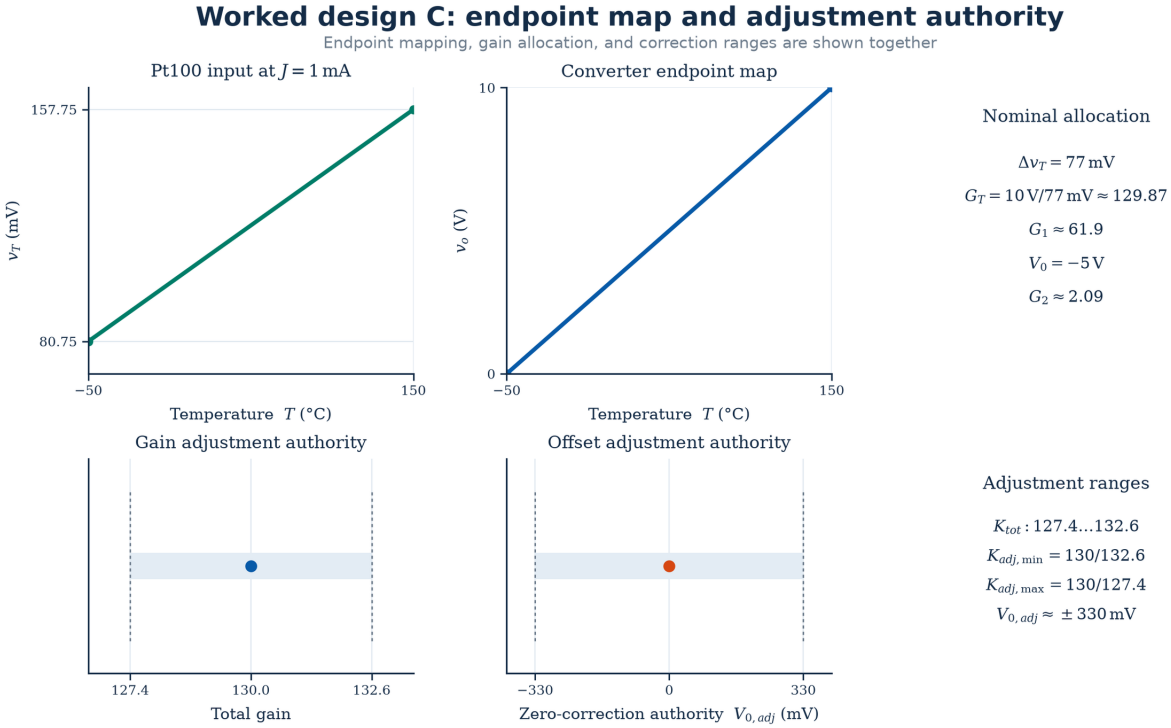


Figure 103. Worked-design endpoint map with separate gain and zero-adjustment authority bands.

9.9.Converter resolution and analogue gain

The converter must provide enough intervals to represent the required physical increment. Over a $200\,^{\circ}\mathrm{C}$ span, a desired increment of $0.5\,^{\circ}\mathrm{C}$ requires at least

$$\frac{200}{0.5} = 400 \tag{253}$$

distinct intervals. The next binary count is 512, corresponding to 9 bits. A 9-bit ideal converter over the full range gives approximately

$$\frac{200}{512} = 0.391\,^{\circ}\mathrm{C/LSB}\,. \tag{254}$$

This code-count argument relates the required physical increment to the minimum number of converter intervals.

10.Output-driving considerations

The output stage must preserve the conditioned voltage under the real load, cable, current, thermal, and stability conditions; balanced transmission improves rejection but does not create galvanic isolation.

10.1.Output stages and transmission

For an A/D converter on the same board or immediately adjacent, a single-ended output is simple and adequate. A remote receiver benefits from a balanced pair feeding a differential input. Ideally, the two conductors carry equal and opposite signal components, so externally coupled common-mode interference is rejected at the receiver and the cable's external field is reduced.

Balanced transmission depends on impedance and amplitude symmetry; it is not guaranteed merely by providing two labelled output pins. Nor does a balanced pair imply zero average voltage in every implementation. The receiver's common-mode range, cable shield termination, source impedance balance, and CMRR over frequency must be specified.

A single-ended high-current buffer can use an inverting unity-gain op-amp stage with complementary emitter followers inside the feedback loop:

$$v_o \simeq - v_{in} . \tag{255}$$

Class-AB pre-bias reduces crossover distortion, while the transistor pair supplies current to the load. The feedback capacitor shown in the circuit introduces a compensation pole.

10.2.Buffer inside the global feedback loop

When an operational amplifier has adequate voltage accuracy but insufficient load current, a current-gain stage with voltage gain approximately one and current gain $A_I \gg 1$ can be added. The booster belongs inside the operational amplifier's global feedback loop. Feedback then senses the actual load voltage after the booster, so the op amp corrects the booster's base-emitter drop and small-signal voltage error.

The closed-loop current-booster arrangement is shown in Figure 104.

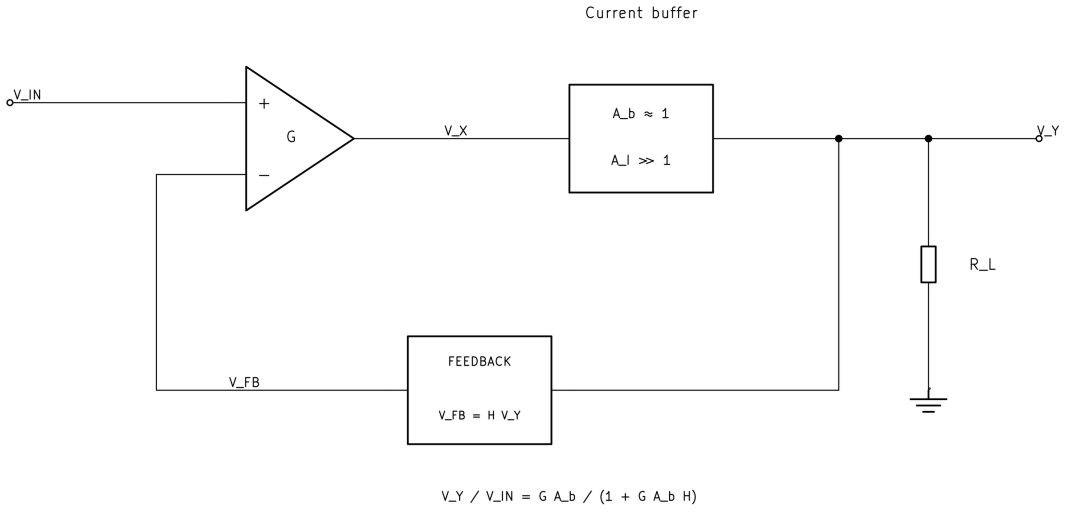


Figure 104. Output-current buffer enclosed by the operational amplifier's global feedback loop.

If the booster voltage gain is $A_b \simeq 1$, the composite open-loop gain is

$$G^* = GA_b \simeq G, \tag{256}$$

while the output-current capability is multiplied. A booster placed outside the loop can supply current, but its voltage error and crossover nonlinearity are not corrected by the preceding op amp.

10.3.Single-transistor emitter follower

A single transistor can extend the current capability when the load requires only one current polarity. Figure 105 shows the PNP version, connected to the negative supply and used for a negative load voltage. The transistor lies inside the feedback loop, so the operational amplifier corrects its base-emitter drop. The mirrored NPN connection supplies positive current.

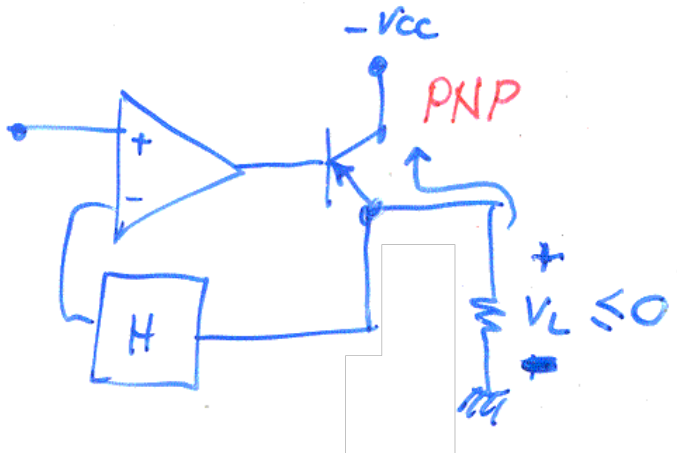


Figure 105. PNP emitter-follower current booster for a negative load voltage, enclosed by global feedback.

In magnitude, the base-emitter voltage difference is approximately one forward junction drop, and the base-current requirement is

$$|V_B - V_L| \simeq V_{BE,\mathrm{on}}, \quad |I_B| \simeq \frac{|I_C|}{h_{FE}}, \quad |I_L| \simeq |I_C|\,. \tag{257}$$

If the operational amplifier can supply the required base-current magnitude $I_{o,\max}$, the approximate current ceiling is

$$|I_L|_{\max} \simeq h_{FE} I_{o,\max}\,. \tag{258}$$

The usable output excursion is also limited by the operational amplifier drive range, the transistor junction drop and the load. The transistor current, dissipation and safe operating region must remain within their limits. One transistor does not provide the bidirectional drive of a complementary pair.

10.4.Complementary class-B output and crossover distortion

To source and sink load current, complementary NPN and PNP emitter followers can be connected in push-pull. With neither transistor prebiased, each begins to conduct only when its base-emitter voltage reaches a threshold V_γ. The simplified transfer is

$$V_y \simeq \begin{cases} V_x - V_\gamma, & V_x > V_\gamma, \\ 0, & |V_x| \le V_\gamma, \\ V_x + V_\gamma, & V_x < -V_\gamma\,. \end{cases} \tag{259}$$

The dead band around zero produces crossover distortion.

The complementary pair is shown in Figure 106; the zero-crossing dead zone follows from the piecewise transfer above.

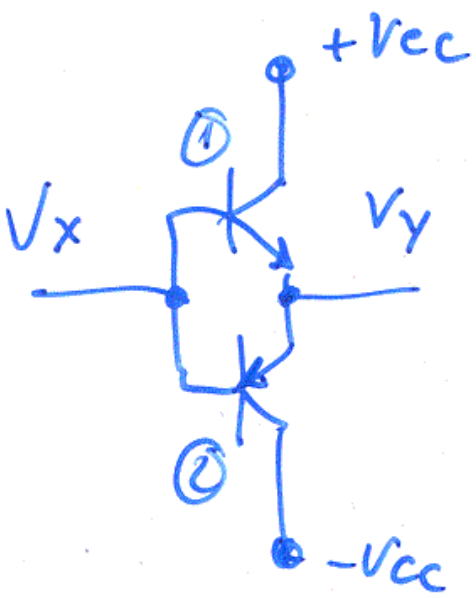


Figure 106. Complementary class-B output pair.

Global feedback can force the final load voltage to follow the command at low frequency, but the operational-amplifier output must slew rapidly across roughly $2V_\gamma$ at each zero crossing. Finite bandwidth and slew rate mean that a dynamic crossover residue can remain.

10.5.Class-AB prebias

The proposed cure is to shift the two transistor base voltages by approximately one junction drop in opposite directions:

$$V_{B,N} = V_x + V_\gamma, \quad V_{B,P} = V_x - V_\gamma \,. \tag{260}$$

Then each emitter approximately reproduces V_x in its active half-cycle, and a small overlap current removes the class-B dead zone. Two forward-biased diodes provide the two required base-emitter level shifts. The result is a class-AB output stage.

The diode-biased class-AB arrangement is shown in Figure 107. The bias resistors R_{B+} and R_{B-} correspond to R_1 and R_2 in the calculations below.

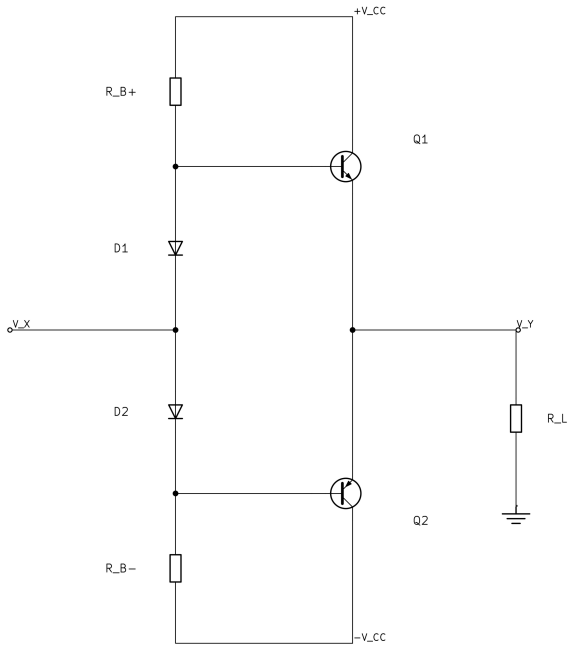


Figure 107. Complementary class-AB output pair with transistor prebias.

Ideal voltage sources are not appropriate diode-bias elements because transistor base currents vary with load. The diodes require a positive bias current even at the worst signal and load condition. Current-source bias provides the clearest model; practical implementations may replace those sources with resistors to the positive and negative supply rails.

At the positive output extreme, a representative calculation uses

$$I_{R1} = \frac{V_{CC} - V_\gamma - V_x}{R_1}, \tag{261}$$

$$I_{D1} = I_{R1} - I_{B1}, \quad I_{D2} = I_{R2}, \tag{262}$$

with a drive-current relation of the form

$$I_x = I_{R2} - I_{R1} + I_{B1}\,. \tag{263}$$

The resistor values must satisfy three competing requirements over both output polarities:

1. diode current must remain positive and sufficiently large to maintain the intended forward drop;
2. enough transistor base current must be available at the minimum expected current gain;
3. the operational-amplifier drive current must remain below its rating.

An illustrative design uses $V_{CC} = 15\ \mathrm{V}$, $V_{L,max} \simeq 10\ \mathrm{V}$, diode current of order 1 mA, base current of order 1 mA, and an op-amp drive target of order 10 mA. A resistance near $1\ \mathrm{k\Omega}$ can demand more than 20 mA, whereas several-kilohm values are more plausible. Final values must be calculated from the selected devices, load, supply range, and temperature limits.

10.6. Quiescent current and thermal stability

The most important limitation of a fixed two-diode bias is that the base-to-base voltage is approximately $2V_\gamma$, while transistor collector current depends exponentially on base-emitter voltage. A small bias excess can therefore make both output transistors conduct simultaneously and produce a large quiescent current from the positive rail to the negative rail.

Emitter resistors R_E introduce local negative feedback. As current rises, the voltage $I_E R_E$ subtracts from the effective base-emitter drive and limits simultaneous conduction. They also aid current sharing and make the quiescent point less sensitive to device differences, at the cost of output voltage and power loss.

The emitter resistors providing local stabilising feedback are shown in Figure 108.

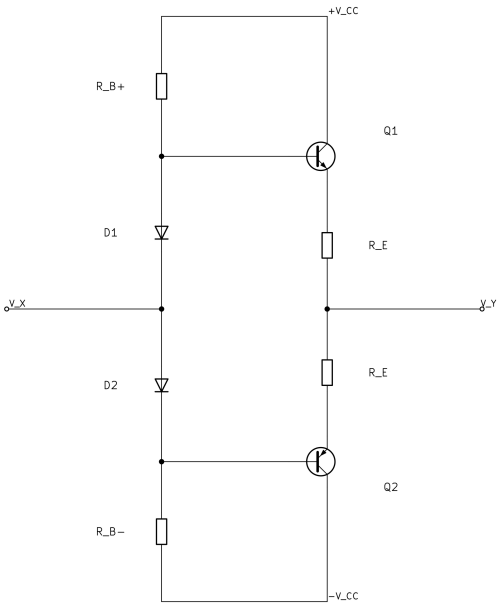


Figure 108. Class-AB output pair with emitter resistors for controlled current sharing and local stabilisation.

At approximately constant collector current, a silicon transistor's V_{BE} decreases by roughly $2.2\ \mathrm{mV/°C}$. With a fixed base-to-base bias, heating therefore tends to increase collector current; increased current causes more power dissipation and more heating. This positive feedback can lead to thermal runaway, which is why the emitter resistors and quiescent-current control are necessary.

11.Study of the ESA universal signal-conditioning board

11.1.Acquisition chain and range mapping

The ESA board is the analogue section between a transducer and acquisition. It accepts the electrical quantity made available by the transducer, applies the required amplification, translation and filtering, and supplies a voltage to the A/D conversion stage. Excitation is part of the same chain whenever the transducer requires a voltage or current supply.

The end-to-end physical-to-numerical path is shown in Figure 109.

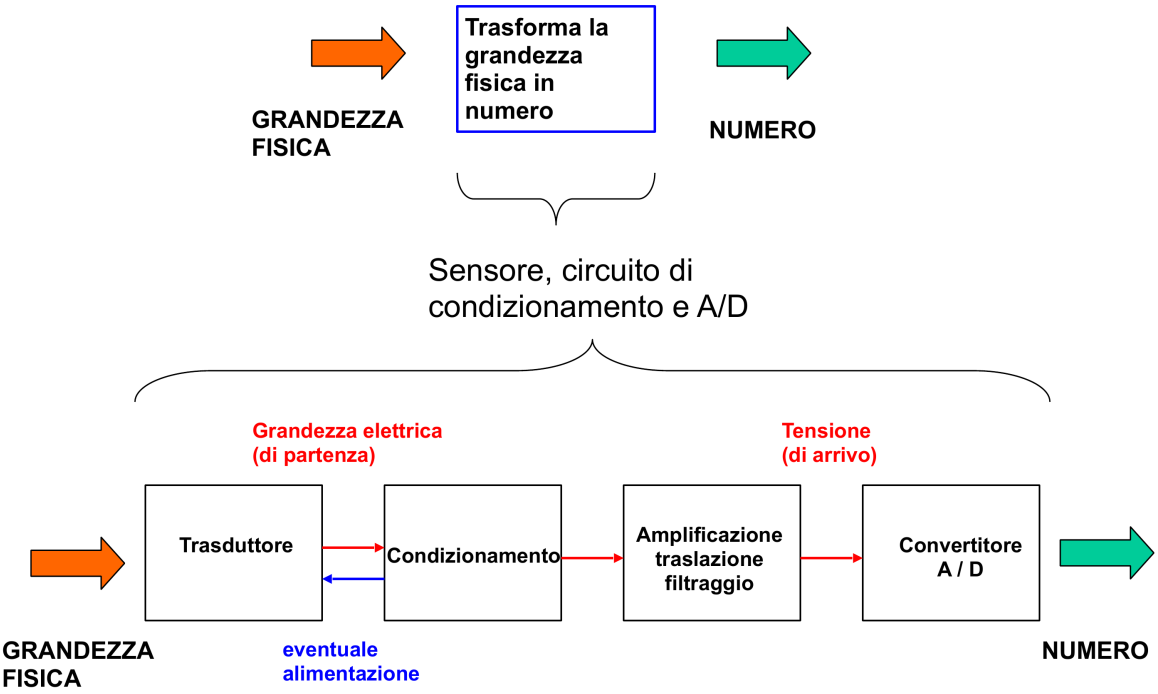


Figure 109. Physical-to-numerical acquisition chain with transduction, excitation, analogue conditioning and A/D conversion.

The board implements the range mapping already derived in Chapter 3 and illustrated in Figure 9. The transducer establishes the electrical endpoints; the selected gain and reference translation place those endpoints within the acquisition range. The Pt100 examples in Chapter 4 and Sections 9.6-9.8 show how excitation, offset removal and distributed gain realise that map without exceeding an intermediate node limit. The following board diagrams identify the physical blocks that perform those previously derived operations.

11.2.Universal architecture and operating sequence

The high-level architecture divides the board into selectable input functions, filtering, staged amplification, reference translation, output delivery and sensor-support resources. The available front ends accommodate charge, voltage, current and differential signals; the resource group provides voltage supply, current supply, current sink, reference voltage and external supply connections as required by the selected interface.

The selectable front ends and shared downstream channel are shown in Figure 110.

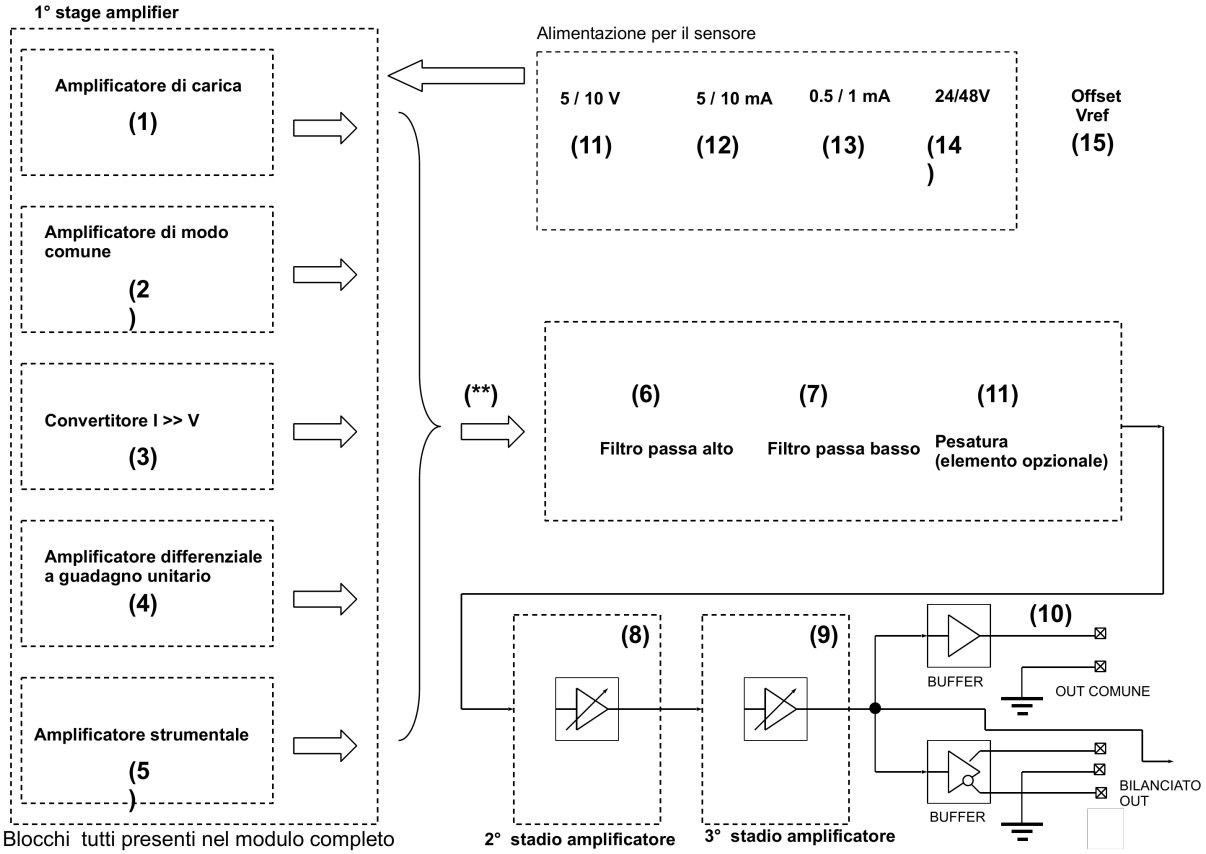


Figure 110. High-level universal conditioning-board architecture with selectable inputs, filters, gain stages, excitation resources and output modes.

The detailed architecture retains a common downstream channel while exposing selectable front-end paths and parallel excitation and reference services. The selectable filter banks precede the later gain stages. Translation is not applied at one arbitrary point: the first reference-derived offset is summed at the output of the first-stage interface, a second reference-derived offset is summed after the second amplification stage, and the final adjustment stage provides the remaining gain and offset trim before the output driver.

The detailed measurement path and its support resources are shown in Figure 111.

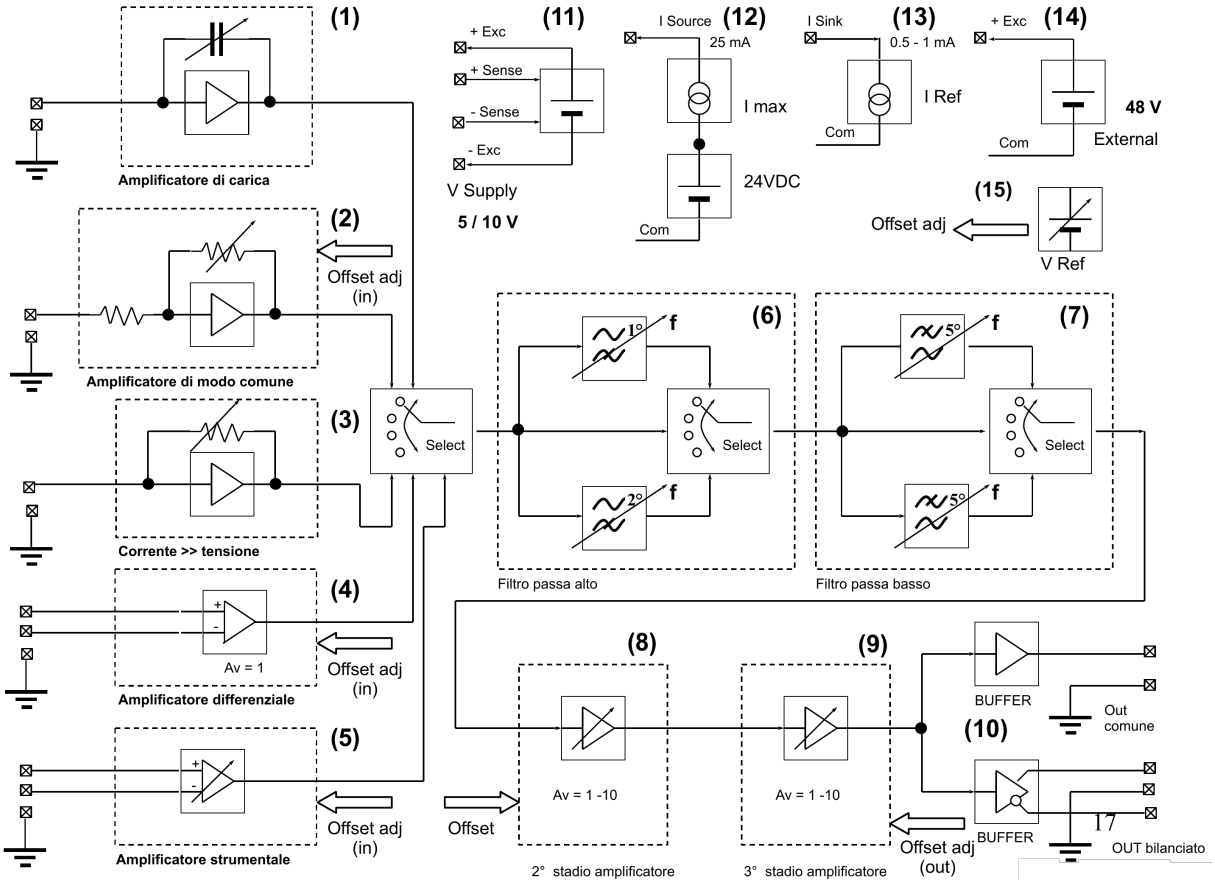


Figure 111. Detailed universal conditioning-board routing with input selection, excitation paths, filter banks, reference insertion and output delivery.

The board supports the input and excitation combinations shown below. Each row states the native transducer quantity entering the selected first-stage function.

Table 4. Supported input and excitation combinations.

Interface family	Board resource	Quantity entering the first stage
Variable resistance or Pt100	Precision current excitation	Voltage across the resistive element
Resistive bridge	5 V or 10 V voltage excitation	Differential voltage
Piezoelectric element	Charge amplifier	Charge
Photodiode	Reverse-voltage bias and current-to-voltage conversion	Current
Two-wire industrial transmitter	24 VDC supply, 25 mA maximum	4–20 mA current
Industrial 0–10 V transmitter	Voltage supply	Voltage
Magnetodynamic sensor	No excitation	AC voltage
Potentiometric sensor	Voltage excitation	Voltage
Limit switch	Voltage excitation	Voltage or current

11.2.1.Ground-referenced voltage input

The ground-referenced voltage input uses a finite input resistance rather than the high input impedance of the instrumentation path. The available termination is described as several kilohms or $50\,\Omega$, allowing a grounded source or signal generator to feed the common downstream channel. The first reference generator can be switched into the summing input to translate the first-stage output before filtering.

The finite-impedance single-ended option is shown in Figure 112.

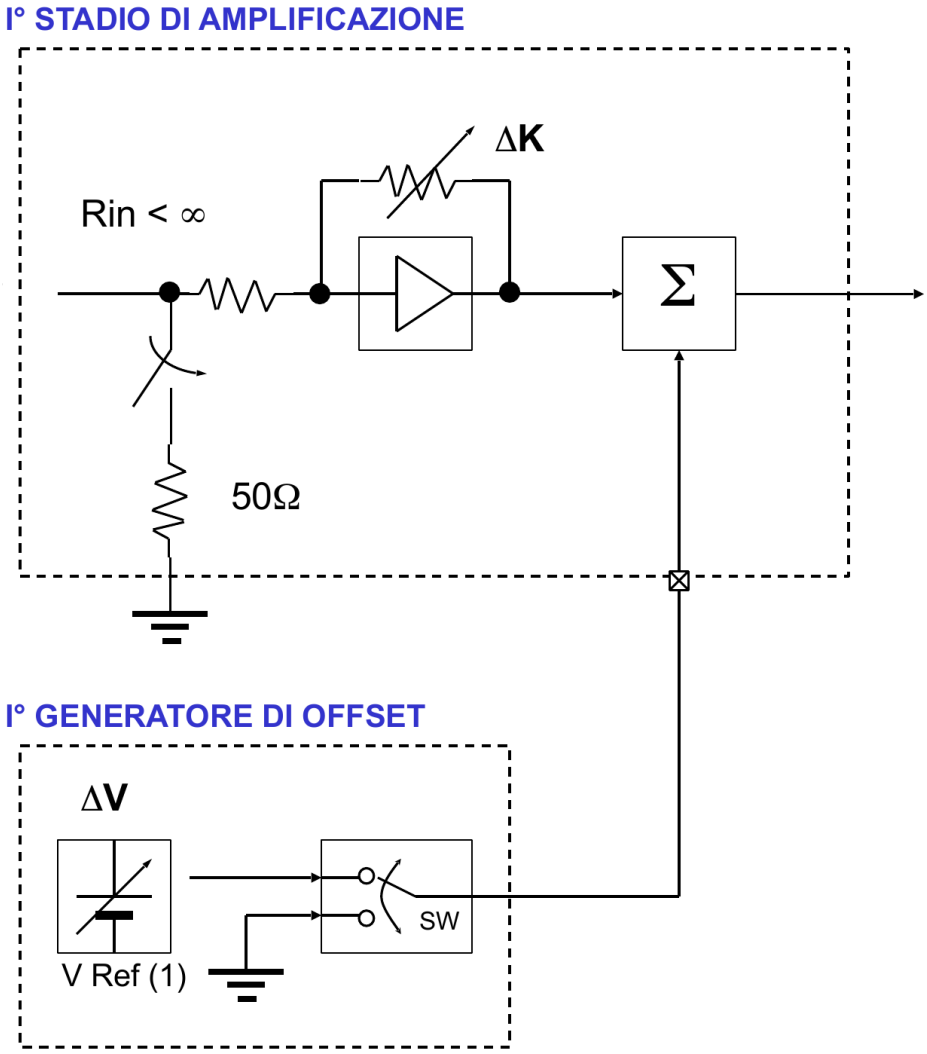


Figure 112. Ground-referenced voltage input with selectable termination, first-stage gain and switchable reference-derived offset insertion.

11.2.2.Current-to-voltage input

The current-input option configures the first stage as a current-to-voltage converter with an input resistance approaching zero. It is intended for current-output transducers such as photodiodes. The separate polarization control shifts the quiescent input potential and can provide reverse bias for a photodiode; it is not an additional signal-gain stage.

The current-input stage and its independent polarization path are shown in Figure 113.

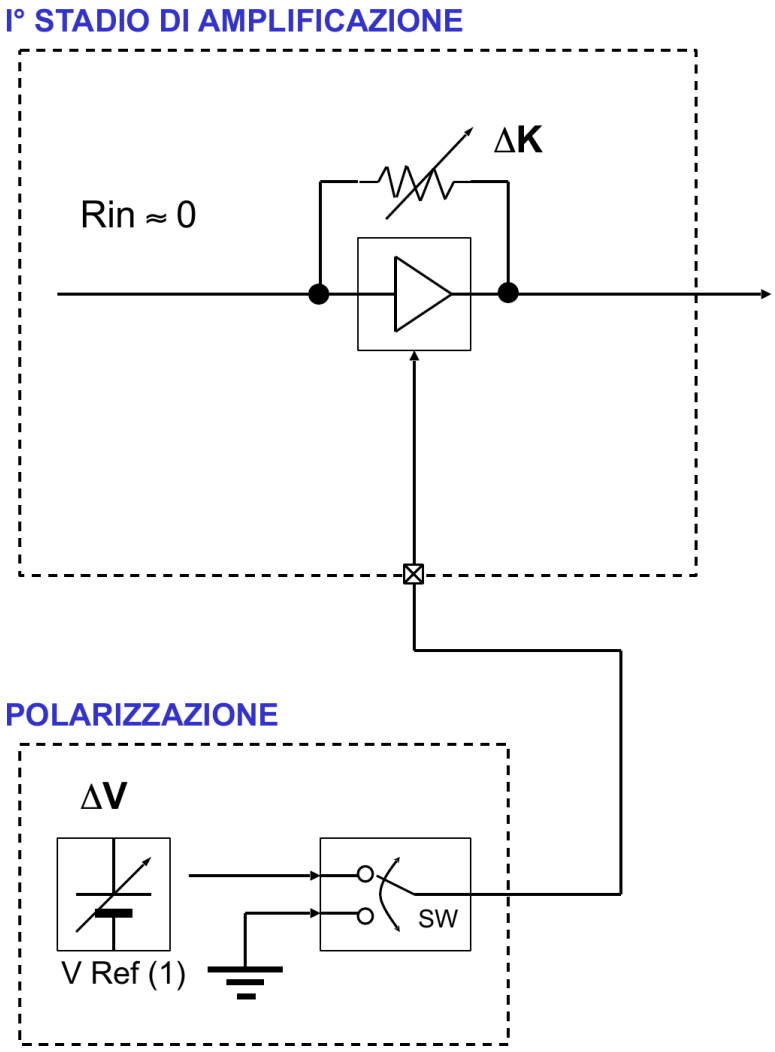


Figure 113. Current-to-voltage first stage with near-zero input resistance and a separately selectable polarization voltage.

11.2.3.Charge-amplifier input

The charge-input option uses a FET-input operational amplifier with low input capacitance. The selectable conversion range stated for this input spans 0.1 to $10\,\mathrm{V/nC}$. The feedback capacitor C_x sets the incremental charge-to-voltage conversion,

$$\Delta V = -\frac{\Delta Q}{C_x}. \tag{264}$$

The illustrated $20\,\mathrm{M\Omega}$ feedback resistor R_f, connected in parallel with C_x, is required to prevent amplifier saturation and is selected to provide a high-pass cut-off of a few hertz. Changing C_x changes the charge-to-voltage conversion factor.

The C_x-R_f feedback network is shown in Figure 114.

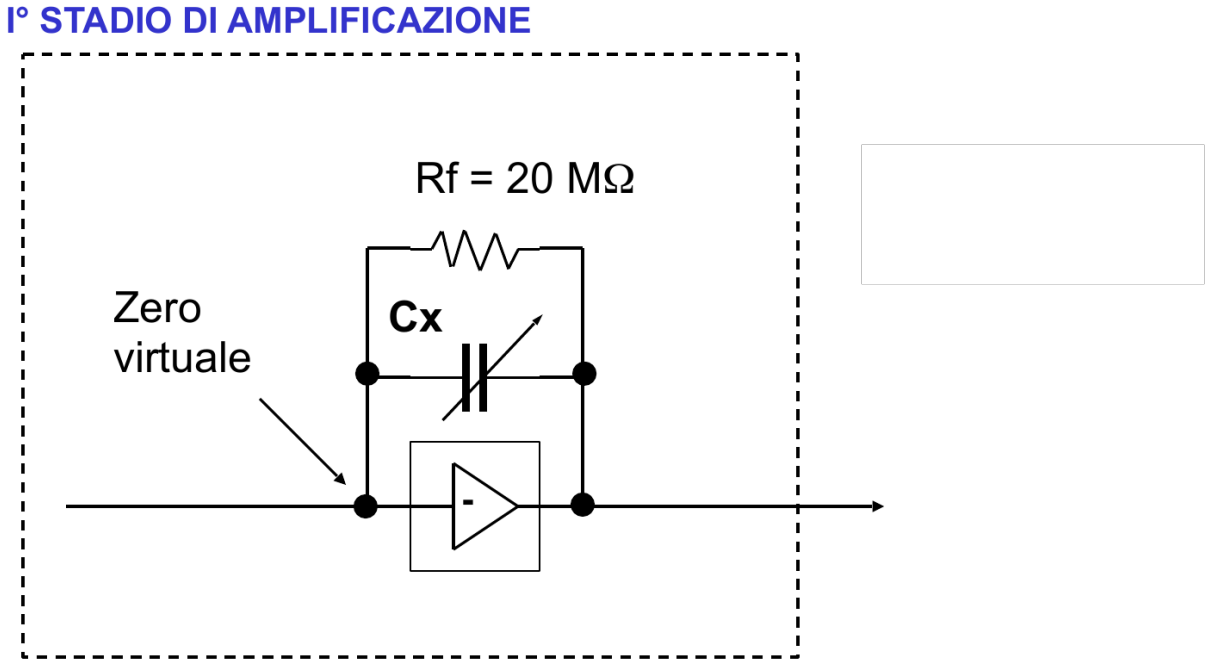


Figure 114. Charge-amplifier first stage with capacitive feedback and a parallel 20 megohm resistor that prevents amplifier saturation.

The complete operating sequence begins with the selected excitation resource and first-stage interface. The first stage performs the required charge, current or voltage conversion and gain; its output is then summed with the first selected reference offset. The translated signal passes through the filter banks and second amplification stage, after which the second selected reference offset is summed. The third amplification stage, independent final gain/offset adjustment and output driver complete the channel in that order.

The complete operating sequence is shown in Figure 115.

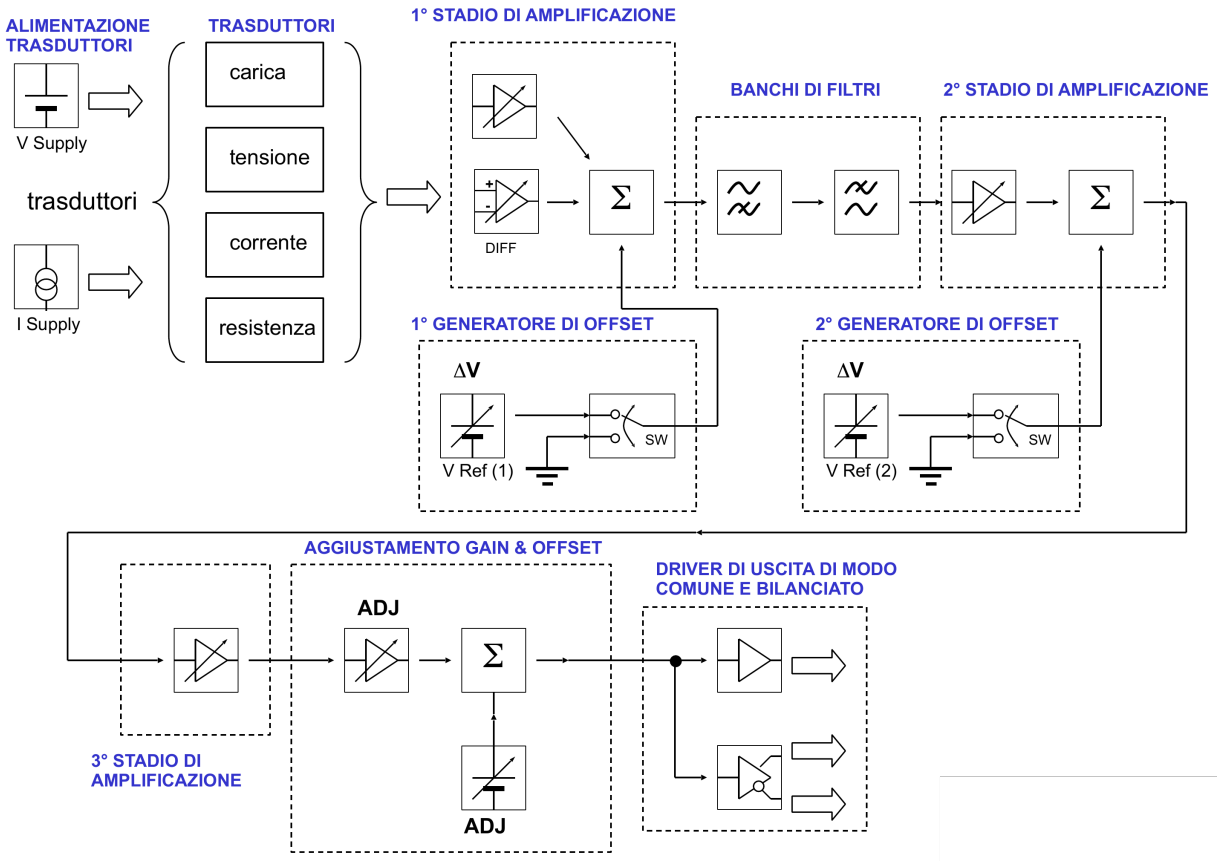


Figure 115. Complete conditioning sequence from sensor supply and input selection through filtering, gain, offset adjustment and output driver.

11.3.Output-mode branch

The final driver has a local single-ended branch and a balanced branch for connection to a differential receiving input. The single-ended path is the local output route; the balanced path carries the conditioned quantity as a differential transmission pair.

The local and balanced output branches are shown in Figure 116.

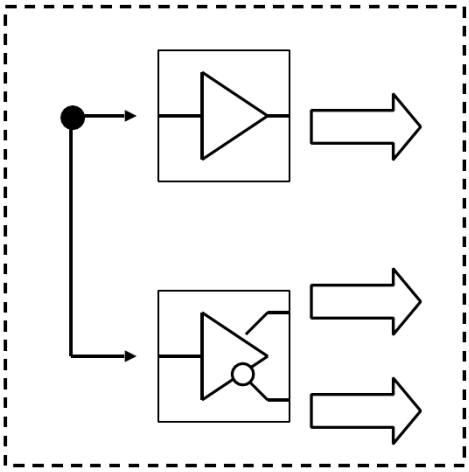


Figure 116. Single-ended and balanced output branch for local acquisition and differential reception.

11.4.Configured sensor routes

11.4.1.Differential-voltage route

A differential-voltage signal enters the first amplification stage and then follows the fully populated filter route shown for this configuration. That route contains the selectable fifth-order low-pass bank followed by two first-order high-pass sections before the second amplification stage. Later gain, gain/offset adjustment and output driving complete the path. The first-stage gain choices shown are 1, 10 and 100, and the complete output relationship is displayed as $V_{out} = (V_{in}K) + V_{ref}$.

The complete differential-voltage route is shown in Figure 117.

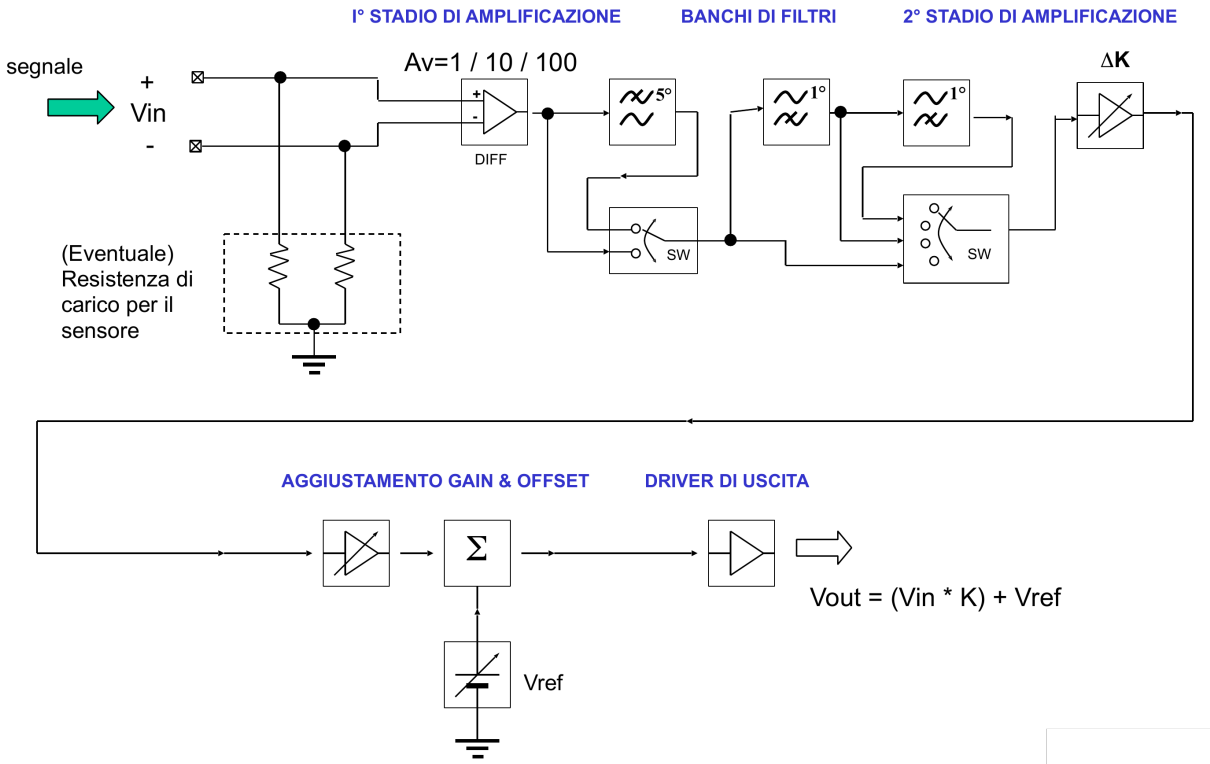


Figure 117. Configured differential-voltage sensor route through the first stage, filters, gain adjustment and output driver.

11.4.2.Ground-referenced voltage route

For a ground-referenced signal, the channel grounds the negative input of the differential first stage and then uses the shared gain, adjustment and output sections. The configured route shown here selects the fifth-order low-pass branch only; unlike the differential route in the preceding figure, it does not show the two first-order high-pass sections in circuit. Test points TP1 through TP4 are placed after the first stage, after the selected filter branch, after the second stage and at the output respectively.

The grounded input and test points TP1 through TP4 are shown in Figure 118.

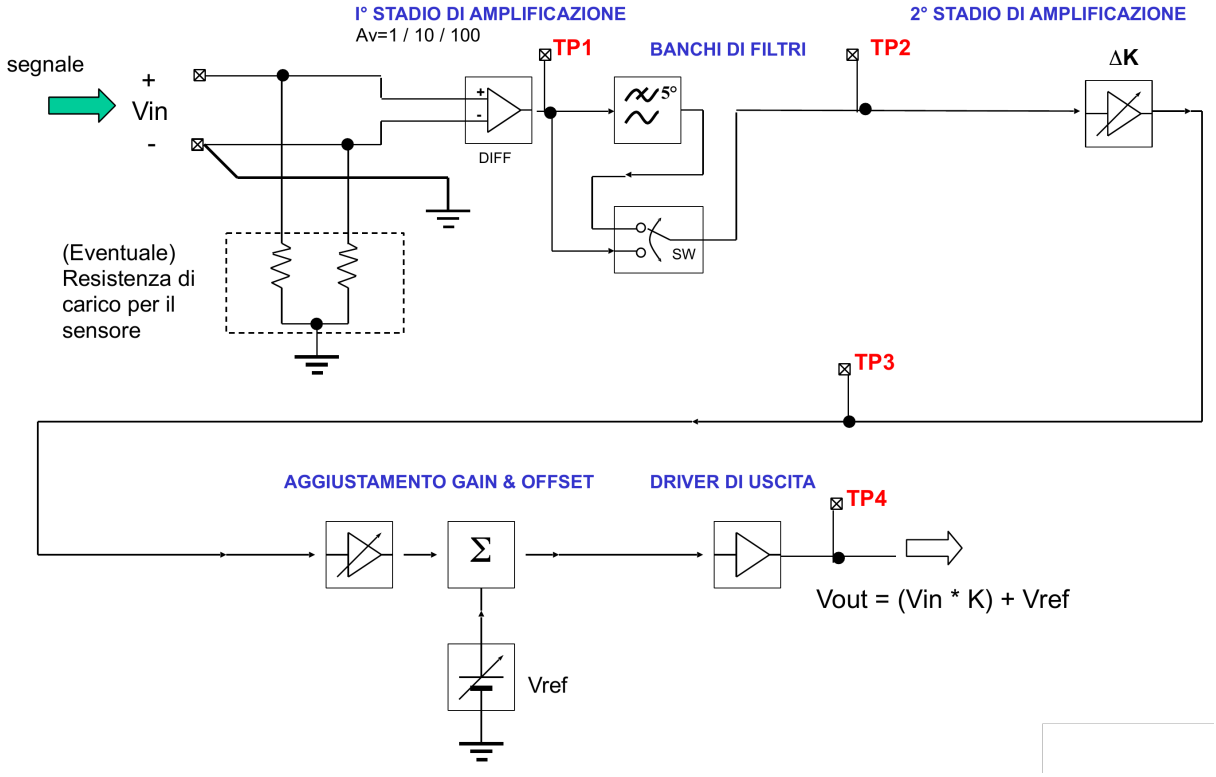


Figure 118. Configured ground-referenced voltage route with test points through the shared conditioning channel.

11.4.3.Four-wire bridge route

A bridge transducer is excited at 5 V or 10 V and read through the high-impedance differential input. The illustrated route uses a typical first-stage gain of 100, followed by selected filtering, later gain, gain/offset adjustment and output driving.

The four-wire bridge route is shown in Figure 119.

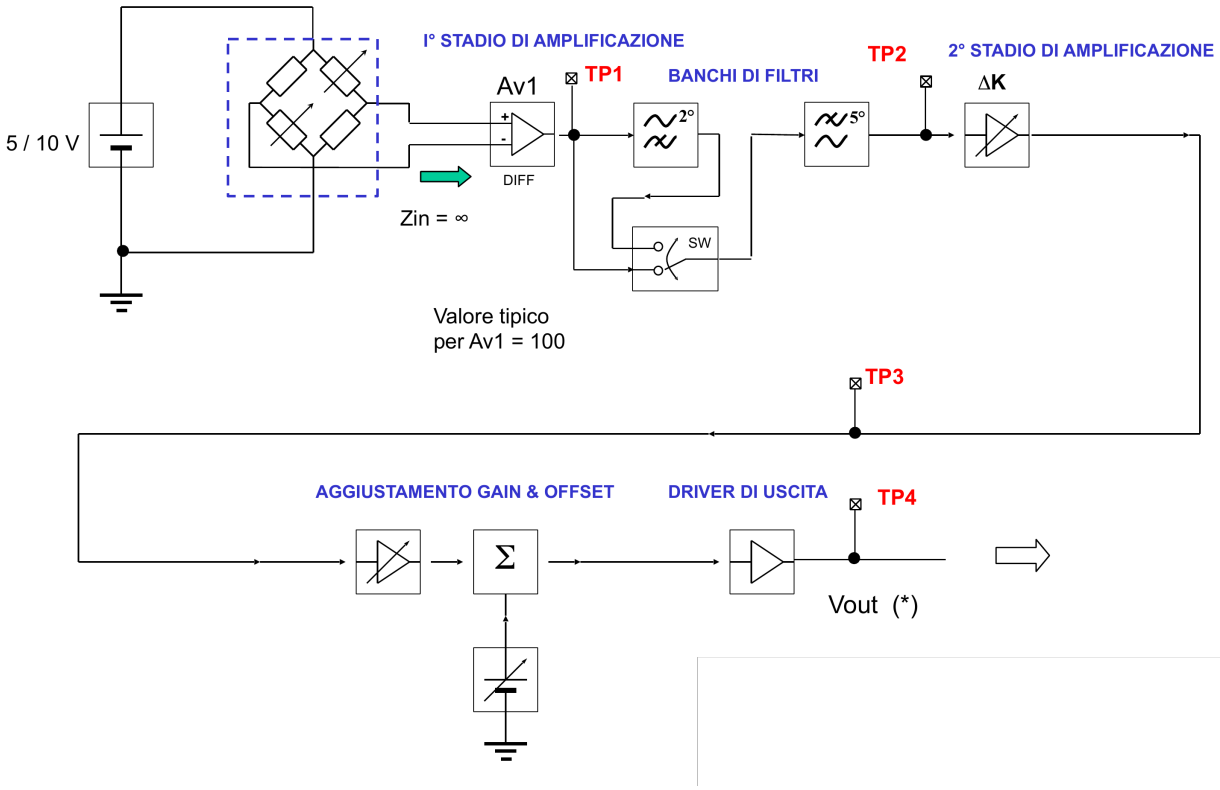


Figure 119. Four-wire bridge-transducer route with 5 V or 10 V excitation, differential input, filtering, adjustment and output.

Note: the output scale depends on the overall gain and the type of transducer. The value 100 identifies a typical first-stage gain; it does not by itself define the complete conversion from the physical quantity to output voltage.

11.4.4.Four-wire Pt100 route

The Pt100 route uses impressed current and separate sensing conductors. The shown configuration applies $I = 0.5\,\mathrm{mA}$, holds the sensing-wire current at approximately zero, uses a differential first stage with $A_v = 100$, introduces a 5 V offset reference, applies the fifth-order low-pass bank and completes the channel with later gain, adjustment and output driving. The displayed output scale is $100\,\mathrm{mV/°C}$, or another selected value.

The complete four-wire Pt100 route is shown in Figure 120.

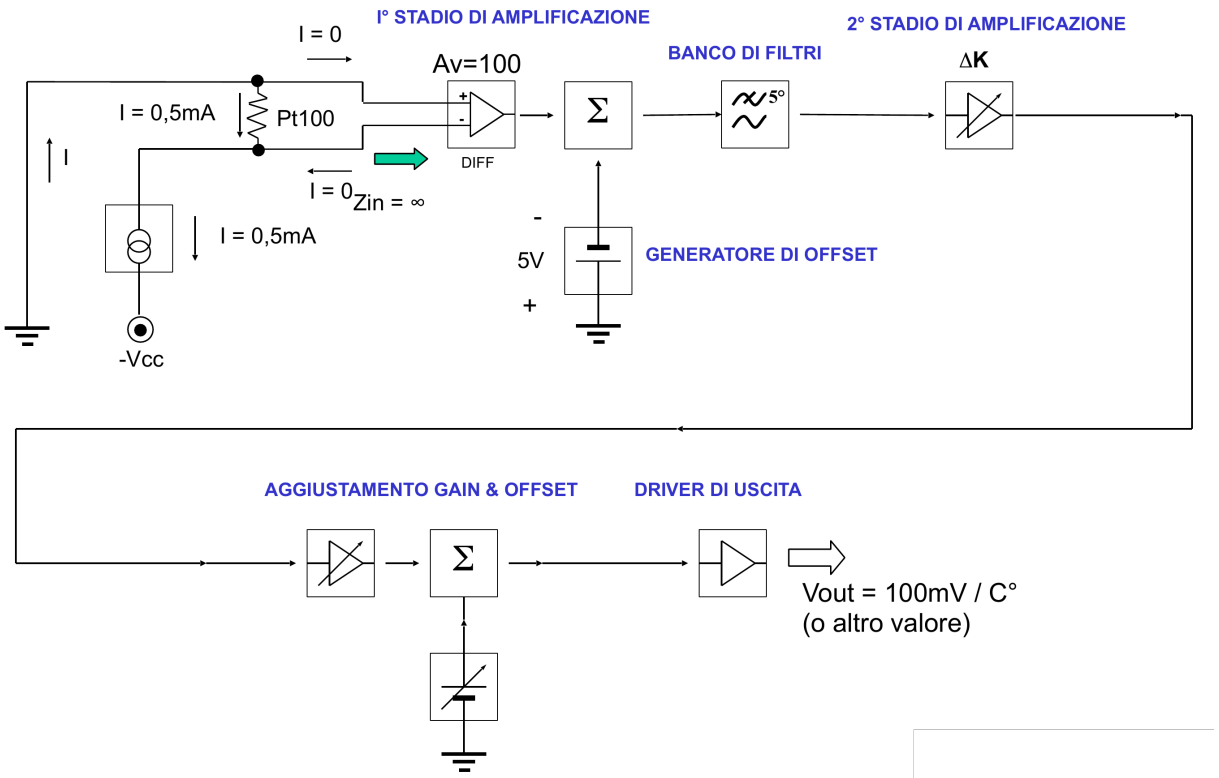


Figure 120. Four-wire Pt100 route with impressed-current excitation, high-impedance sensing, differential gain, offset, low-pass filtering and scaled output.

11.5.External input and differential front-end circuits

The external-input circuit in Figure 121 applies the RF suppression and overload protection studied in Section 5.8. The series resistor and shunt capacitor attenuate radio-frequency pickup before it reaches the active front end. Low-leakage diodes connect the node to the positive and negative Zener reference branches during an overvoltage.

The RC filter and bidirectional clamp are shown in Figure 121.

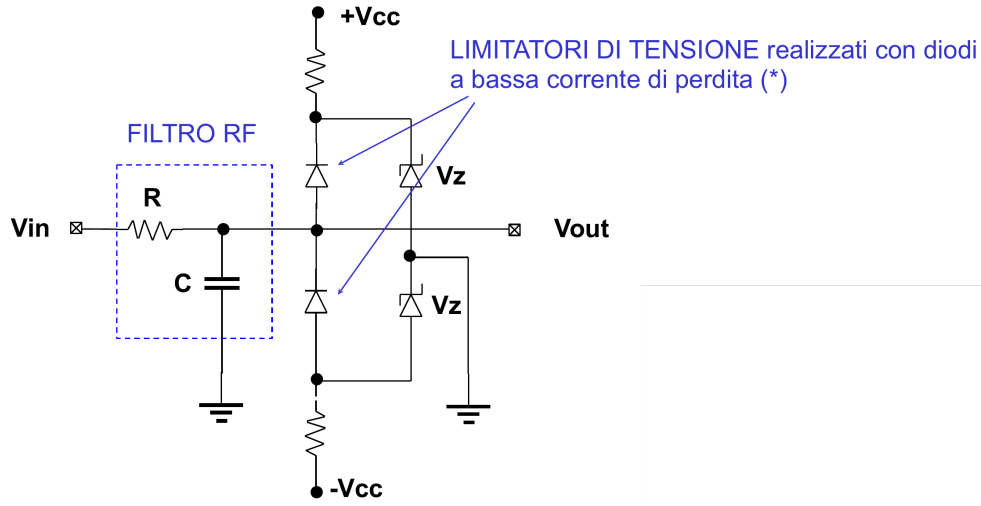


Figure 121. Input RF filter and bidirectional diode-Zener voltage-limiting circuit.

Note: the maximum clamped voltage magnitude is approximately the sum of one diode forward threshold and the Zener voltage. Typical Zener values in this circuit are 10-12 V and must remain below the supply magnitude. The series resistor limits the current delivered to the clamp.

$$V_{\text{clamp},+} \simeq V_Z + V_F, \quad V_{\text{clamp},-} \simeq -(V_Z + V_F)\,. \tag{265}$$

The high-impedance instrumentation input uses the three-amplifier structure studied in Section 8.3. Its reference input translates the output after differential amplification. The switch changes the resistance linking the two first-stage feedback networks, while the matched R_2 output network subtracts their voltages with unity gain. Figure 122 shows the two gain-setting resistances R_{v1} and R_{v2}.

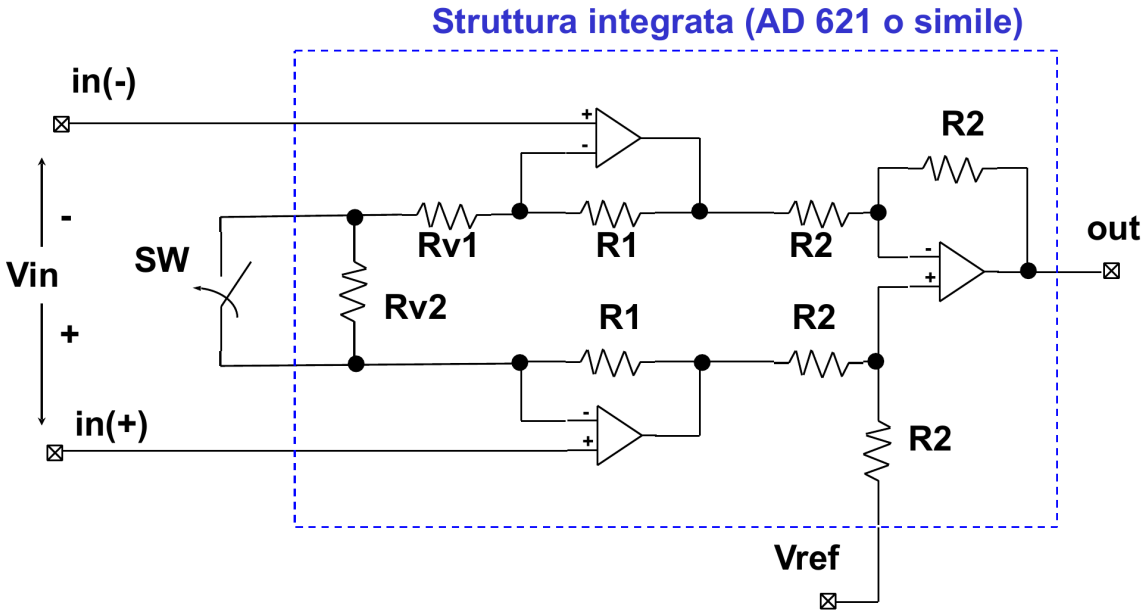


Figure 122. High-impedance instrumentation-amplifier input with reference translation and switch-selectable gain path.

With the switch closed, R_{v2} is bypassed and the output is

$$V_{\text{out}} = \left(1 + \frac{2R_1}{R_{v1}}\right) V_{\text{in}} + V_{\text{ref}}\,. \tag{266}$$

With the switch open, the two resistances are in series:

$$V_{\text{out}} = \left(1 + \frac{2R_1}{R_{v1} + R_{v2}}\right) V_{\text{in}} + V_{\text{ref}}\,. \tag{267}$$

For the stated AD621 configuration, these settings give differential gains of 100 and 10 respectively. The gain is $(V_{\text{out}} - V_{\text{ref}})/V_{\text{in}}$; the simpler ratio $V_{\text{out}}/V_{\text{in}}$ applies only when the reference term is zero. The AD620 population provides the unity-gain alternative described for the board.

An alternative population uses a resistor-ratio differential amplifier. Four equal resistors give unity differential gain; when $R_3 > R_2$, the illustrated relationship is $V_{out} = V_{in}(R_3/R_2)$.

The resistor-ratio alternative is shown in Figure 123.

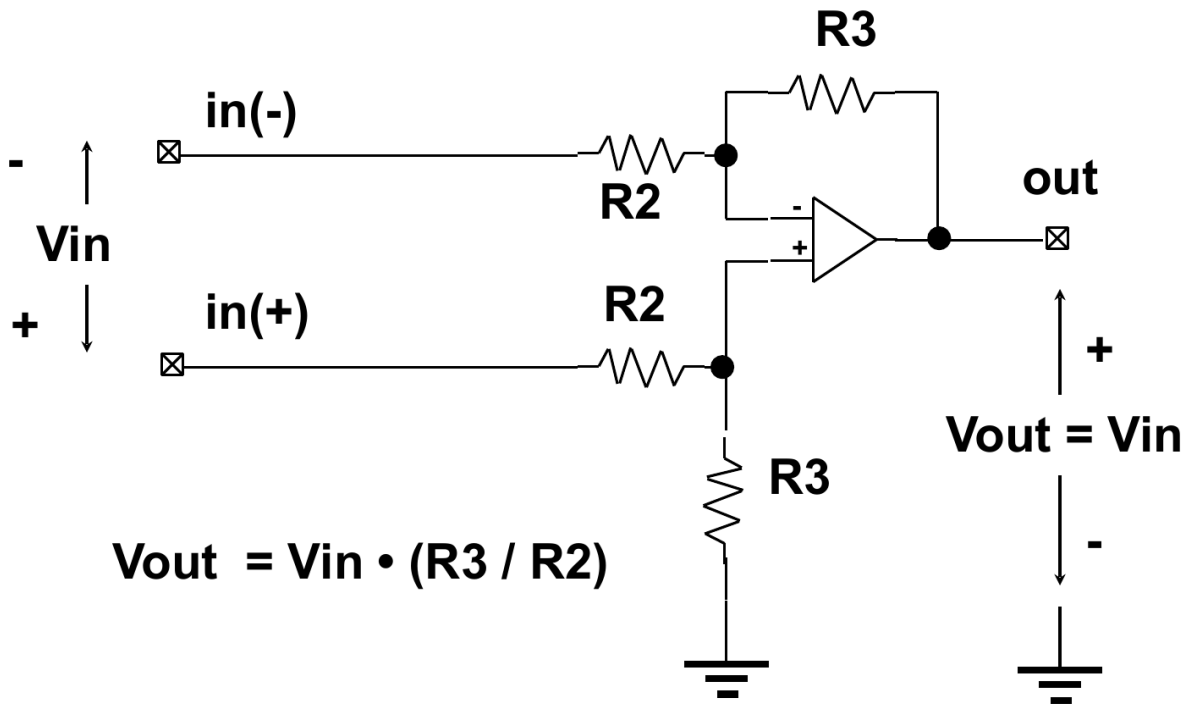


Figure 123. Resistor-ratio differential amplifier covering unity and higher-gain alternatives.

11.6.Excitation circuits

The voltage-excitation circuit uses two force conductors and two sense conductors so that feedback is taken at the remote load. The board provides selectable 5 or $10\,\mathrm{V}$ excitation and a $50\,\mathrm{mA}$ current limit. The diagram states $V_{out} = V_{in}$ for $R_1 = R_2 = R_3 = R_4$ under the indicated condition $R_f \ll R_1$; the shunt branch provides an indication related to load current.

The four-wire remote-sense connection is shown in Figure 124.

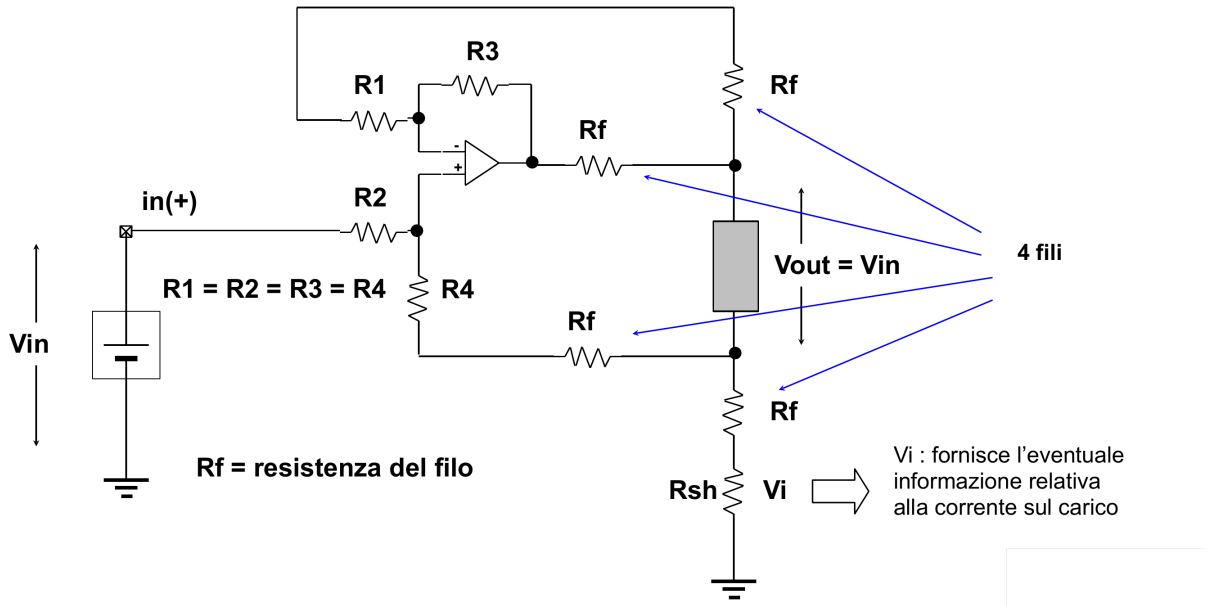


Figure 124. Four-wire remote-sense voltage-excitation circuit with remote feedback and load-current shunt branch.

The extended voltage-excitation circuit adds a transistor output path and a current-sense resistor. Its indicated limit is $I_{max} = 0.6\,\mathrm{V}/R_{sh}$, while the remote-sense feedback arrangement and the condition $R_f \ll R_1$ remain in place.

The pass-transistor and shunt-limited extension are shown in Figure 125.

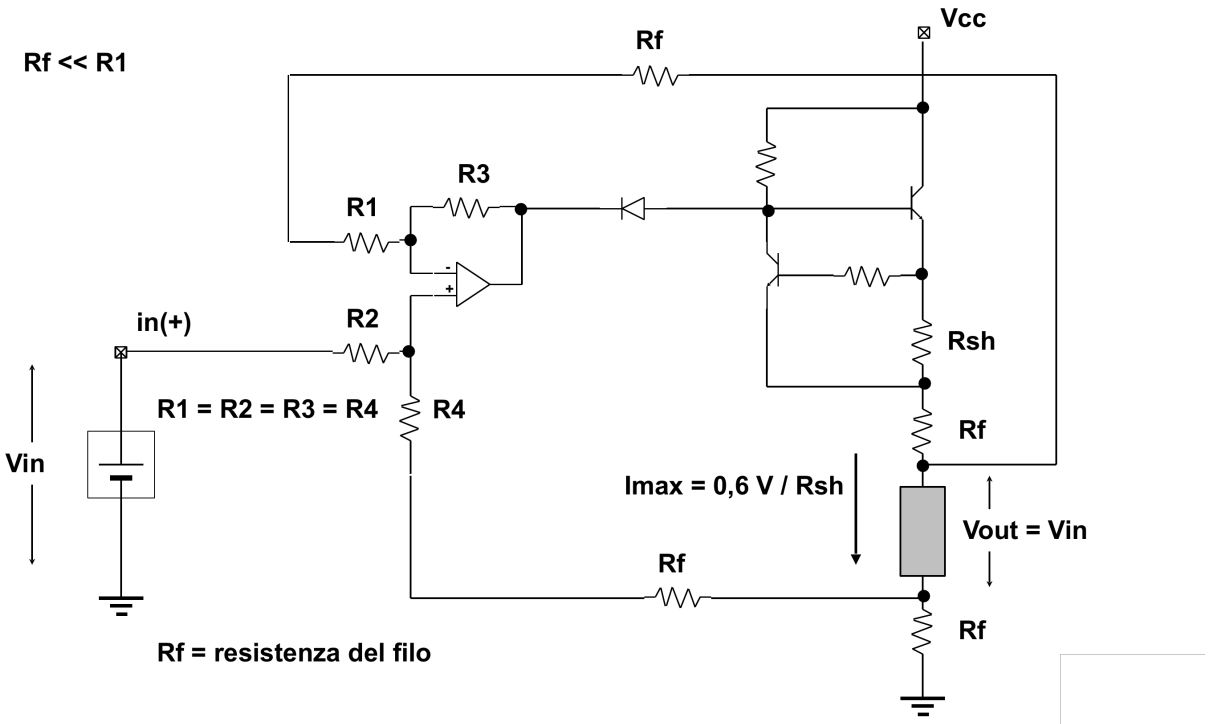


Figure 125. Remote-sense voltage-excitation circuit with transistor current boost and shunt-defined current limit.

The precision current-excitation path is a current sink for resistive sensors. A 5 V reference, operational amplifier, MOSFET and $10\,\mathrm{k\Omega}$ sense resistor establish $I_D = I_S = V_{in}/R_{sh}$. The nominal current is 0.5 mA, with 1 mA also selectable.

The MOSFET current sink is shown in Figure 126.

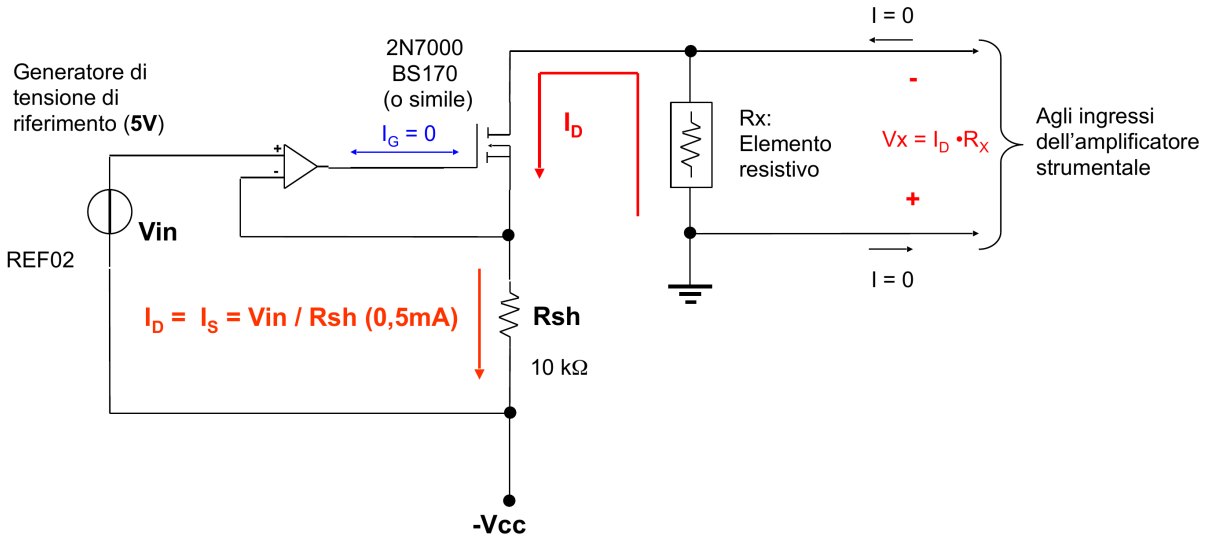


Figure 126. Precision MOSFET current-sink excitation circuit for a resistive sensor.

11.6.1.Additional supply and reference resources

Additional board resources include a $24\,\mathrm{VDC}$ supply rated at a maximum of $25\,\mathrm{mA}$ for two-wire $4\text{-}20\,\mathrm{mA}$ transmitters, an external $48\,\mathrm{V}$ supply connection for condenser microphones and a separate voltage-reference generator for offset compensation.

11.7.Filter banks

The detailed high-pass implementation comprises two cascaded first-order RC cells isolated by unity-gain FET-input buffers. Its selection network provides bypass, one-cell first-order operation or two-cell second-order operation. The two-cell path has an indicated maximum slope of 12 dB per octave, and the available corner-frequency range extends from millihertz values to kilohertz values.

The bypass, first-order and second-order selections are shown in Figure 127.

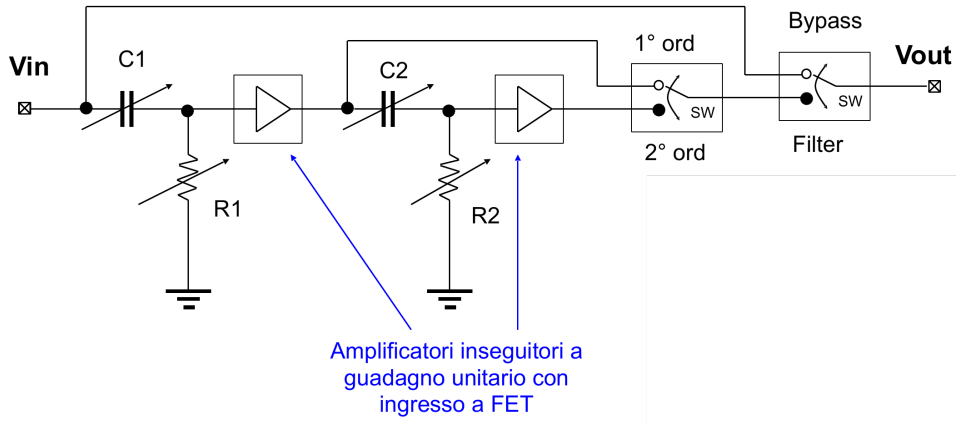


Figure 127. Selectable high-pass implementation with bypass, one buffered RC cell or two buffered RC cells in cascade.

Note: FET-input followers allow very large values of R_1 and R_2, up to approximately 10 megaohms in the illustrated implementation. Large resistances provide time constants of several seconds with non-polarised polyester capacitors. This accommodates signal polarity reversal without relying on a polarised electrolytic capacitor. The small input current is essential when such high resistances are used.

This is the same bypass, one-cell and two-cell structure analysed in Section 6.12 and Figure 79. It controls the lower edge of the measurement band; anti-alias rejection at the upper edge remains the low-pass bank's task. A third-order high-pass belongs to a different module configuration and is not realised by this two-cell circuit.

Figure 128 repeats the fifth-order low-pass topology studied in Section 6.10 and Figure 69, now in its board-level context. The five capacitors provide the energy-storage elements, the equal resistor array scales the characteristic frequencies, and the two FET-input followers provide the active buffered feedback used by the Sallen-Key sections.

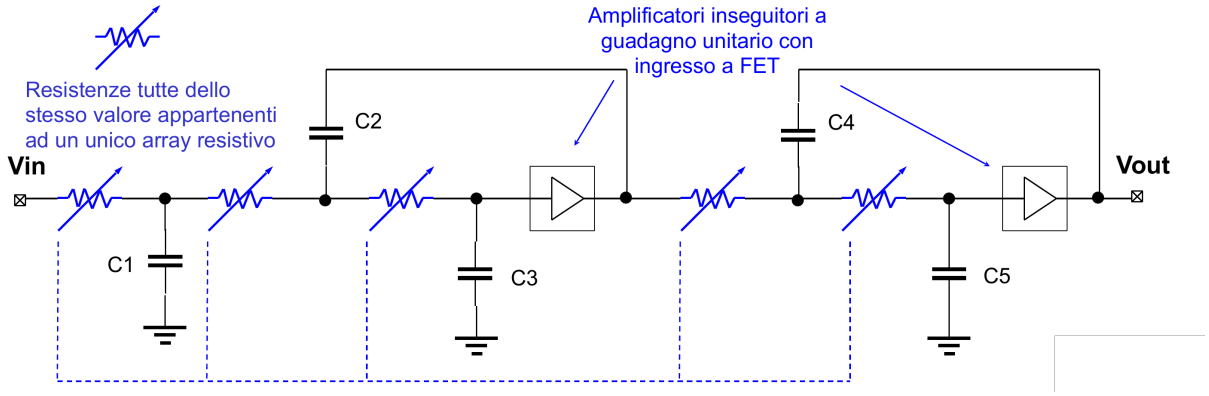


Figure 128. Fifth-order active low-pass bank with a common resistor array, five capacitors and unity-gain follower stages.

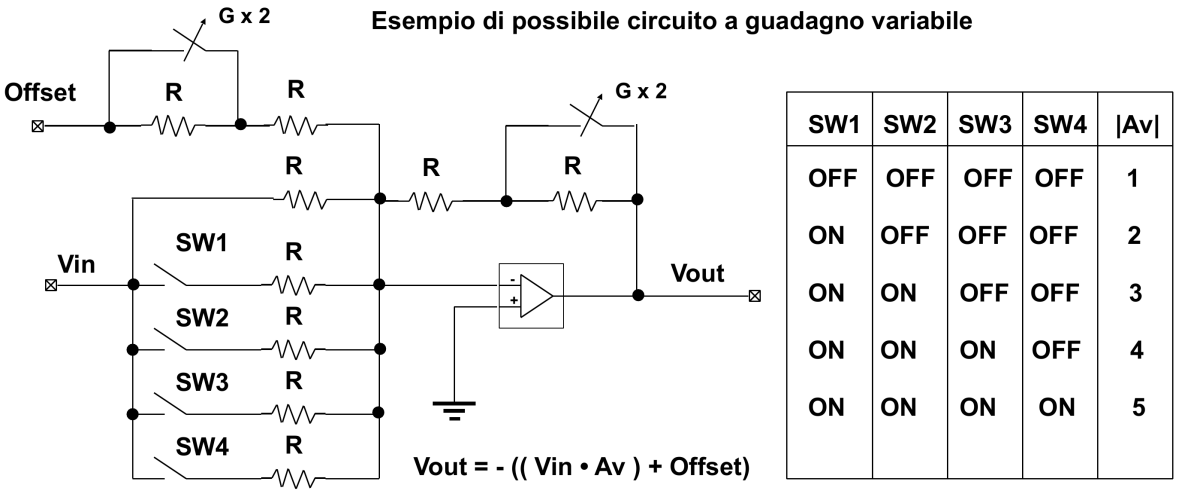
The signal therefore passes through the same RC filtering and unity-feedback building blocks already analysed. Changing all array resistances by the same factor shifts the frequency scale inversely while retaining the intended pole alignment, provided loading and amplifier bandwidth remain negligible. Changing the capacitor ratios selects the Bessel, Butterworth or Chebyshev alignment described in Section 6.11.

At DC the capacitors are open circuits and the followers give nominal unity voltage gain. The Bessel choice favours transient fidelity; its anti-alias adequacy still depends on the stopband attenuation required at the selected sampling rate. The measured comparison in Figures 70-78 supplies the corresponding amplitude and time-response evidence.

11.8.Intermediate gain and final adjustment circuits

The switched inverting stage combines integer gain selection and offset insertion. Four switches provide five defined configurations: all switches open gives $|A_v| = 1$, and closing the switches cumulatively gives $|A_v| = 2, 3, 4$ and 5. The output expression is $V_{out} = -((V_{in}A_v) + Offset)$. The inverting topology also permits a response pole to be introduced, including when the stage is set to unity gain.

The switched gain/offset network is shown in Figure 129.



SW1	SW2	SW3	SW4	|Av|
OFF	OFF	OFF	OFF	1
ON	OFF	OFF	OFF	2
ON	ON	OFF	OFF	3
ON	ON	ON	OFF	4
ON	ON	ON	ON	5

Figure 129. Switch-selected inverting gain and offset stage with gains from one to five.

Two equal-resistor non-inverting alternatives provide fixed gains of two and five, with $V_{out} = 2V_{in}$ and $V_{out} = 5V_{in}$, respectively.

The two fixed-gain alternatives are shown in Figure 130.

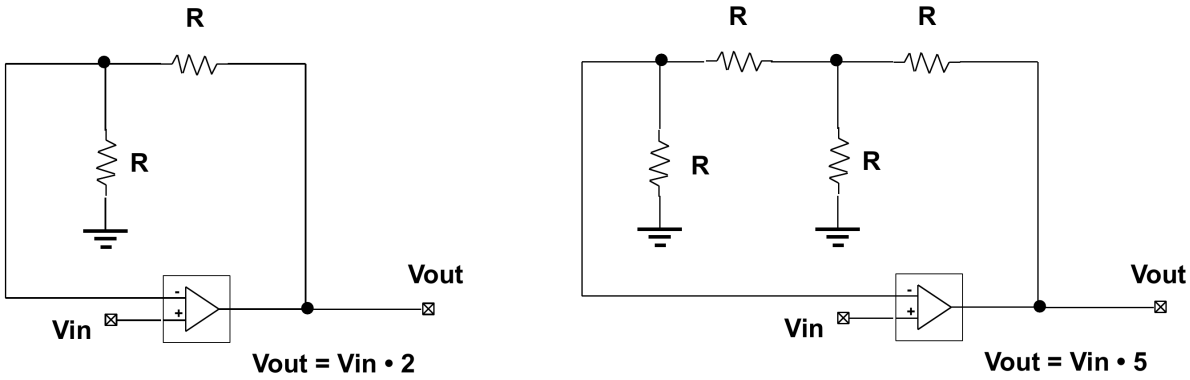


Figure 130. Equal-resistor non-inverting gain alternatives with fixed gains of two and five.

The final adjustment stage in Figure 131 is the weighted inverting summer developed in Section 9.3.3. The signal reaches the virtual-ground node through $R_2 + R_{V2}$; the adjustable offset voltage reaches it through R_1. Both input currents return through the fixed feedback network.

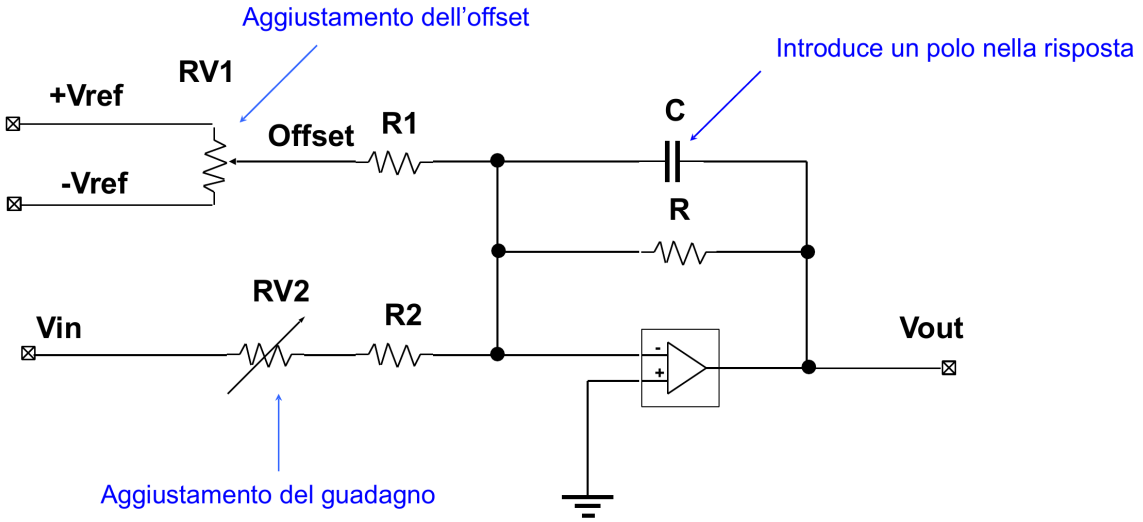


Figure 131. Final weighted inverting summer with independent gain and offset adjustment.

At frequencies low enough for the feedback capacitor to be treated as open, Kirchhoff's current law gives

$$V_{\text{out}} = -\frac{R}{R_2 + R_{V2}} V_{\text{in}} - \frac{R}{R_1} V_{\text{off}} \,. \tag{268}$$

The first term is the adjustable signal gain. Increasing R_{V2} decreases its magnitude. The second term translates the output: R_{V1} moves the offset potentiometer wiper between the positive and negative references, changing V_{off} without changing the fixed feedback resistance. Both contributions are inverted because they enter the inverting summing node.

Using $R_{V1} \ll R_1$ limits loading of the offset potentiometer, while $R_{V2} \ll R_2$ makes the gain adjustment a fine correction about a stable fixed-resistor value. The controls then mainly affect separate affine coefficients, although a practical two-point calibration still checks their residual interaction.

The capacitor C is in parallel with R, so it gives the feedback impedance $Z_f(s) = R/(1 + sRC)$. The frequency-dependent result is

$$V_{\text{out}}(s) = -\frac{R}{1 + sRC}\left[\frac{V_{\text{in}}(s)}{R_2 + R_{V2}} + \frac{V_{\text{off}}(s)}{R_1}\right], \quad f_p = \frac{1}{2\pi RC} \,. \tag{269}$$

This pole limits the high-frequency response of the adjustment stage. Its location must remain compatible with the useful measurement band and the filter-bank settings.

11.9.Single-ended output buffer

The single-ended output buffer combines an inverting operational amplifier with a complementary class-AB transistor voltage follower. The push-pull stage provides sufficient output current for demanding loads such as long cables with capacitance of several nanofarads. The feedback capacitor introduces a response pole to increase the stability margin as the load varies. The displayed voltage relationship is $V_{out} = - V_{in}$.

The compensated class-AB output stage is shown in Figure 132.

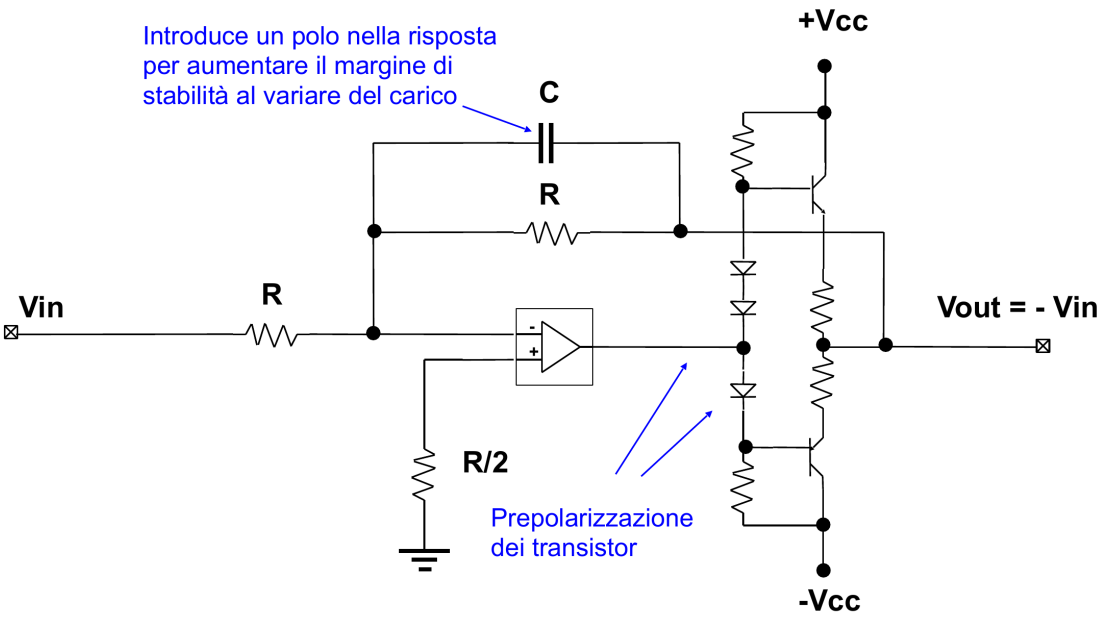


Figure 132. Single-ended class-AB output buffer with inverting amplifier, complementary voltage follower and compensation pole.

11.10.Physical board and complete signal path

The populated ESA board brings the selectable front end, excitation resources, filter banks, gain and offset stages and output driver onto one physical assembly. The illustrated configuration is assigned to a four-wire Pt100 channel.

The populated board used for this Pt100 configuration is shown in Figure 133.

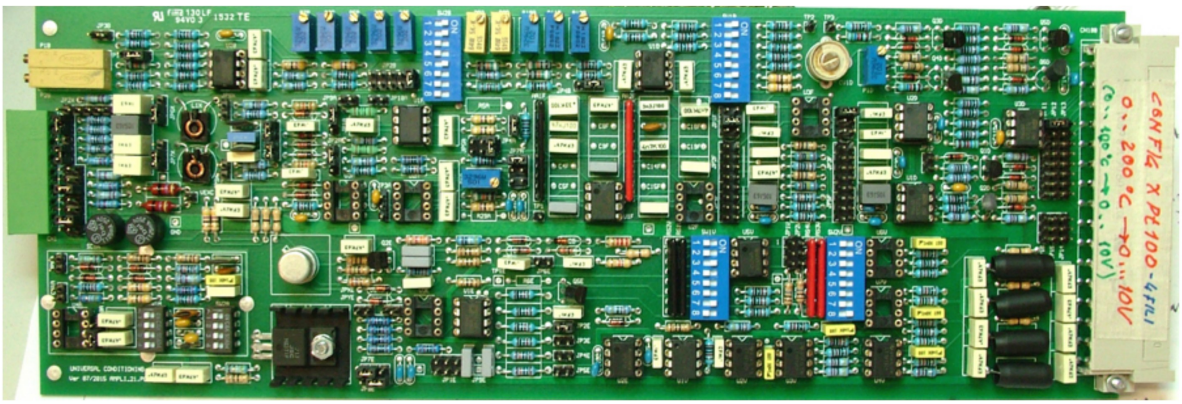


Figure 133. Populated ESA conditioning board configured for a four-wire Pt100 channel.

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